SPICE Parameter Extraction and RO Validation of a 65nm SOI Technology

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Introduction

Accurate extraction of the SPICE model parameter is critical in the CMOS IC design. However, it faces difficult issues in state-of-the-art MOSFET technology. First, the gate *CV* parameter extraction is challenging due to small values and many extrinsic components that need to be de-embedded [1]. Second, the systematic offset of the gate critical dimension (CD) exists between test structures and circuits, introducing a significant uncertainty. Thus, it is not uncommon that the validation of a circuit-level SPICE model involves arbitrary adjustments of capacitance parameters that undermine the confidence level of the model parameters. This paper presents seamless methodologies to resolve these issues. Circuit-level validation of the methodology is given for 65nm PD-SOI ring oscillators (ROs), covering a wide range of simulation conditions.

De-embedding Parasitic Gate Capacitance

This paper proposes to use the same *RC* extractor and technology file as used in actual circuit extractions instead of TCAD field solvers or extra measured data. Equations (1) – (5) describe the proposed de-embedding method. C_{pad} is measured from the difference between the total gate capacitance (C_{gg}) and the gate-to-source/drain capacitance (C_{gc}) of the DUT at strong inversion. The sum of all other extrinsic components (C_{ext}) is the difference in C_{gc} simulation between the netlist with fully-extracted extrinsic *C*'s ($C_{gc,full\text{-}C}$) and an ideal LVS netlist without extrinsic *C*'s ($C_{gc,LVS}$), as noted in Eq. (2).

$$C_{pad} = C_{gg,orig} - C_{gc,orig} \text{ at strong inversion} \quad (1)$$

$$C_{ext} = \left(C_{cont} + C_{wire} + C_{of2}\right) = C_{gc,full-C} - C_{gc,LVS} \quad (2)$$

$$C_{gg} = C_{gg,orig} - C_{ext} - C_{pad} \quad (3)$$

$$C_{gc} = C_{gc,orig} - C_{ext} \quad (4)$$

$$C_{gb} = C_{gb,orig} - C_{pad} \quad (5)$$

One of the major sources of the error in circuit simulation is the ambiguous definition of the intrinsic MOSFET portion. Unfortunately, it is very difficult to estimate the boundaries from measurement or simulation since some of them are solely subject to the *RC* extractor. The main advantage of the proposed methodology is to share the same platform with the circuit netlist extraction, being inherently conscious of the boundary between the intrinsic and extrinsic portions.

The most ambiguous component is the outer-fringe capacitance (C_{of}=C_{of1}+C_{of2}) of the gate to the source/drain active region, since it is quite common that the *RC* extractor adds a portion (C_{of2}) of the outer-fringe capacitance in the netlist to capture any layout variants, yet its amount is often neither explicit nor physical.

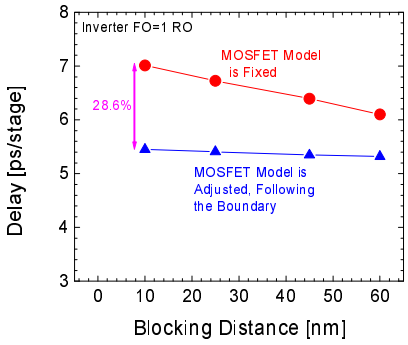

Fig. 1. Impact of outer-fringe capacitance on circuit switching delay, comparing the same C_{of} case with same C_{of1} case.

It is noteworthy that high accuracy in MOSFET model alone does not necessarily lead to high accuracy in circuit simulation, due to possible inaccuracies in the circuit-layout *RC* extractor. Figure 1 demonstrates that the switching delay can be maintained within ±1.2% error when the intrinsic capacitance (C_{int}) is adjusted to cope with the change in extrinsic (C_{ext}). Contrarily, when the MOSFET model is extracted without accounting for the boundary condition (assuming C_{ext}≈0), it shows up to 28.6% error – potentially even more – due to double counting C_{ext} (predominantly C_{of2}).

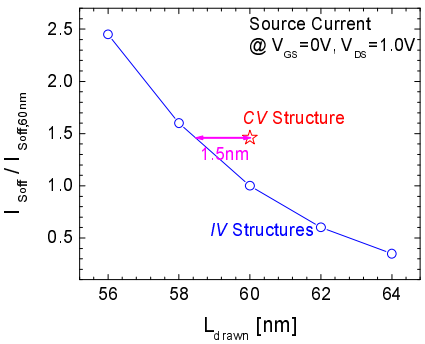

Fig. 2. Channel off current trend for different drawn lengths from *IV* structures compared with the off current of the CV structure.

Synchronizing Gate CD between *IV* and *CV*

It is difficult to maintain the exact same gate CD between *IV* and *CV* test structures due to the distance and drastic difference in the structural density and size. Measuring an absolute gate CD is a challenging task, but estimating its relative difference between two MOSFETs can be a lot easier. Figure 2 compares I_{Soff}/W of the *CV* structure with I_{Soff}/W trend of the *IV* structure. The I_{Soff}/W of the *CV* structure with 60nm drawn length matches to that of the *IV* structure with 58.5nm drawn

length, thus the gate CD offset is 1.5nm. This offset and its corresponding threshold shift have to be reflected into the originally fitted *CV* model parameters before circuit-level validation.

Circuit-Level Validation

The proposed capacitance parameter extraction flow was applied to the BSIMSOI SPICE model extraction of a 65nm PD-SOI technology. The switching delay and dynamic and static currents of RO were measured, then compared with SPICE simulation results. To get the pseudo-dynamic steady state, an indirect body initialization (IBI) technique was applied [2].

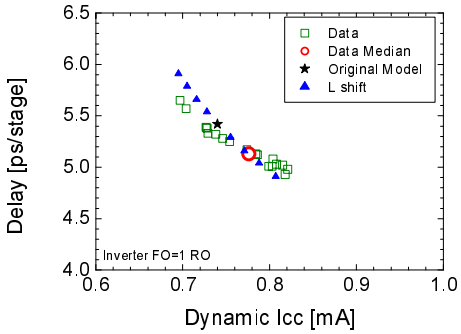

Fig. 3. An inverter FO=1 ring oscillator delay vs. power supply current, comparing measured data with simulation results.

The as-extracted model in Fig. 3 was off from the data median by 5.7% in an inverter FO=1 RO delay. A gate offset was applied in simulations, varying by a 2nm incremental step. The best model-to-silicon agreement was obtained for 2.3nm gate CD offset between the *IV*/*CV* extraction structures and this RO.

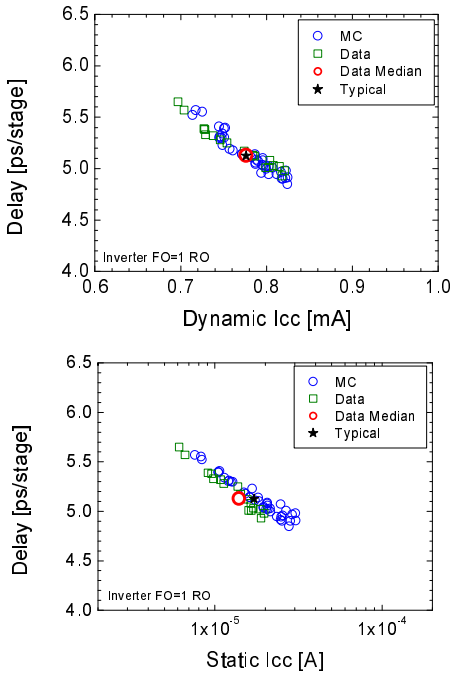

Fig. 4. Monte Carlo simulation results of the inverter FO=1 RO compared with the measured data.

After implementing this CD offset in the model, the simulation delay showed 0.08% and 1.9% errors at the same dynamic/static currents, respectively. Figure 4 demonstrates that Monte Carlo simulation can reproduce the measured data distribution very well.

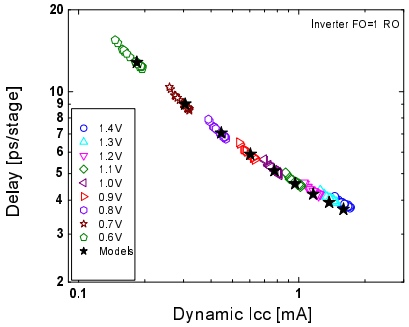

Fig. 5. Inverter FO=1 RO simulation results compared with data for 0.6~1.4V of V_{DD} range at 25°C.

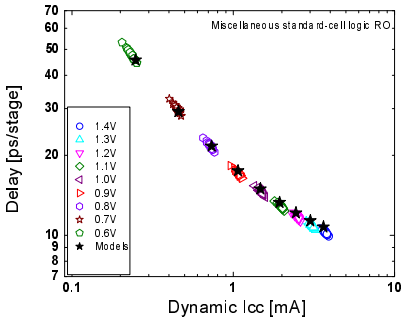

Fig. 6. Miscellaneous standard-cell logic RO (consisting of various standard-cell logic gates such as inverter, NAND, NOR, multiplexer, and flip-flop) simulation results compared with data for 0.6~1.4V of V_{DD} range at 25°C (after 1.55nm gate CD correction).

Figures 5 and 6 validate simulation results of two ROs. A similar level of agreement was obtained for at 0ºC and 100ºC.

Conclusion

Two major issues in the parameter extraction of the short-channel MOSFET gate capacitance are parasitic capacitance removal and uncertainty of the gate CD. The parasitic is defined by the *RC* extractor; thus, this paper proposes to use the same *RC* extractor for model extraction and circuit simulation. The systematic gate CD offset between structures can be estimated from transistor's I_{Soff}/W versus L trend and RO's delay vs. dynamic current. Excellent agreements were obtained in 65nm PD-SOI RO model-to-silicon comparison.

Acknowledgments

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