On Idlow with Emphasis on Speculative SPICE Modeling

Qiang Chen, Zhi-Yuan Wu, Ali B. Icel, Jung-Suk Goo, Srinath Krishnan, Ciby Thuruthiyil, Niraj Subba, Sushant Suryagandh, Judy X. An, Tran Ly, Martin Radwin, James Yonemura, and Farzin Assad

Advanced Micro Devices
One AMD Place, MS 79, Sunnyvale CA 94088-3453, USA, qiang.chen@amd.com

ABSTRACT

An empirical correlation model of I_{dlow}, the MOSFET drain current measured at $V_{gs}=V_{dd}/2$ and $V_{ds}=V_{dd}$, where V_{dd} is the supply voltage, is proposed based on the alpha-power law model. It enables a comprehensive analysis of I_{dlow} over a wide range of device geometry, supply voltage, and temperature in multi-threshold-voltage technologies. Built upon and verified by electrical-test data of 90nm partially-depleted (PD) silicon-on-insulator (SOI) technologies, the newly developed methodology provides practical and efficient guidelines to device target projection and target-based speculative SPICE model extraction.

Keywords: alpha-power law model, Idlow, SPICE, compact model

1 INTRODUCTION

As a first-order assessment of MOSFET inverter delay, the figure of merit CV_{dd}/I has been widely used, where C is the load capacitance (usually of an identical inverter stage), V_{dd} is the supply voltage, and the MOSFET ON current (I_{dsat}) is conventionally chosen for I. It has been shown recently, however, that an effective current (I_{deff}) is more relevant to and better suited for inverter delay estimation, particularly in light of non-uniform scaling (due to oxide thickness and threshold voltage) and transport enhancement techniques [1]. In a simplified formulation, I_{deff} is constructed as the average of two drain currents, I_{dhigh} (at $V_{gs}=V_{dd}$ and $V_{ds}=V_{dd}/2$) and I_{dlow} (at $V_{gs}=V_{dd}/2$ and $V_{ds}=V_{dd}$). The rationale of the I_{deff} approach can be comprehended by studying the load line (i.e., output trajectory) at a given stage of an inverter chain and its relationship to DC I-V characteristics of the component FETs, as illustrated in Figure 1.

Both I_{dhigh} and I_{dlow}, as a result of their immediate importance to circuit performance, have become highly desired specifications for speculative compact models used in digital applications. A speculative compact model (also variably called evaluation-level or guess model) is a SPICE model that is extracted based on targets as opposed to silicon-based models. While the latter are necessary and extremely helpful for model-technology realignment and circuit design debug, speculative models are arguably more important and more pervasive in the state-of-the-art microprocessor sector where technology and designs are executed in parallel (rather than sequentially) according to a pre-defined roadmap. Because of the forward-looking nature of technology and its immaturity at the time of model extraction, targets for speculative models are often generated based on the latest available silicon data through extrapolation and/or certain expectations of technological impact. To ensure desired geometric dependences, targets are typically provided for the nominal-gate-length devices and devices of adjacent gate lengths.

As microprocessor designs advance to meet the low power/low voltage requirements of mobile computing and achieve the best possible performance-per-watt metric for high-performance systems, speculative compact models are required to match device targets across an extensive range of supply voltage. The increasing complexity of targets in conjunction with possible model equation deficiencies makes it necessary to have close model-target interactions and iterations in order to ensure the quality of resulting speculative models.

Despite considerable target projection and model extraction efforts, however, it is sometimes observed that the model-to-target I_{dlow} accuracy is among the lowest, with the difference occasionally reaching tens percent. The inaccuracy is also seen to vary considerably depending on the supply voltage and gate length. Although engineering tradeoff is always an option to somewhat improve the I_{dlow} fit, it noticeably prolongs model extraction time. More importantly, it creates additional uncertainties in model behavior, leading to potential model-to-model and cross-technology-node discrepancies that adversely affect design effort and decisions.

In this paper, a holistic approach is proposed to analyze I_{dlow}, taking advantage of its intimate relationship to other device parameters. Section 2 describes an empirical mathematical model concerning I_{dlow}, followed by its comparison to and verification by electrical-test data of 90nm partially-depleted (PD) silicon-on-insulator (SOI) technologies in Section 3. Its applications toward device targeting and speculative modeling are also discussed.

2 EMPIRICAL I_{DLOW}/I_{DSAT} VS. V_{TSAT}/V_{DD} CORRELATION MODEL

The drain current of short-channel MOSFETs is shown to be proportional to the gate overdrive raised to the power of alpha, known as the alpha-power law model [2],

$$I_d \propto \left(V_{gs} - V_T\right)^{\alpha} \tag{1}$$

where V_T is the threshold voltage. The exponent α is an indicator of mobility degradation at high fields (i.e., velocity-saturation) [3]. Equation (1) recovers to the classic long-channel square-law model when α is set to 2, and approaches the ballistic transport case when α is equal

to unity. A typical value of α for sub-micron technologies has been estimated to be around 1.3 [4].

Recognizing that the I_{dlow} and I_{dsat} bias conditions lead to the same saturation threshold voltage (V_{tsat}), the I_{dlow}/I_{dsat} ratio can be conveniently written as,

$$\frac{I_{dlow}}{I_{dsat}} = \left[1 - \frac{1}{2}\left(1 - \frac{V_{tsat}}{V_{dd}}\right)^{-1}\right]^{\alpha} \quad (2)$$

The above direct proportionality, however, fails to materialize when being applied to silicon measurement data over extensive ranges of V_{dd} and device geometries, possibly because of oversimplification and extrinsic factors such as parasitic resistances. As a remedy while still retaining the physical insight offered by the alpha-power law model, a general correlation instead is searched for between the I_{dlow}/I_{dsat} ratio and a compound variable, X, constructed based on (2),

$$\frac{I_{dlow}}{I_{dsat}} = f(X) \quad (3)$$

where

$$X = \left[1 + A(T - 25)\right]\left[1 + B(V_{dd} - 1)\right]\left[1 - \frac{1}{2}\left(1 - \frac{V_{tsat}}{V_{dd}}\right)^{-1}\right]^{\alpha} \quad (4)$$

The parameters *A* and *B* in the first two terms are introduced to account for the additional temperature and supply voltage dependences that otherwise would be missed. Their values are determined so that the I_{dlow}/I_{dsat} ratio and X do establish a functional relationship, i.e., one-to-one correspondence. Generally, the parameter *A* is relatively insignificant (on the order of 10^{-4} K^{-1}), and *B* is less than unity.

As can be seen in (4), the newly proposed approach treats I_{dlow} holistically in the context of supply voltage, saturation threshold voltage, and the ON current, the last two of which themselves are strong functions of gate length and supply voltage. Consequently, the new approach will enable a comprehensive analysis of I_{dlow} across wide ranges of device geometry and supply voltage needed for target projection and speculative modeling.

3 RESULTS AND DISCUSSIONS

The proposed approach is applied to electrical-test data of 90nm PD SOI technologies. An example is shown in Figure 2 with data collected for the regular-threshold-voltage (regular-Vt) PMOS of varying drawn gate lengths (nominal ± 8nm), sweeping supply voltages (from 0.6V through 1.5 V), and at different temperatures (25 and 100 ^{o}C). The lower end of the correlation curve represents data of lower V_{dd} and/or larger V_{tsat}, while the higher end corresponds to data of higher V_{dd} and/or smaller V_{tsat}.

Similar, tightly distributed correlations are obtained as well for high-threshold-voltage (high-Vt) and low-threshold-voltage (low-Vt) devices of both N and P polarities. It is noteworthy that, when the methodology is applied to high-Vt devices, a deviating trend can sometimes be observed for the very low V_{dd} of 0.6V, as demonstrated in Figure 3. Such deviation is explained by the close proximity between V_{tsat} (corresponding to V_{dd}=0.6V) and V_{gs} at which I_{dlow} is measured (i.e., $V_{dd}/2$=0.3V). Under such conditions, I_{dlow} actually falls into the weak or moderate inversion region, and depends on V_{tsat} or gate overdrive in an exponential fashion rather than by the power law. As a result, analytical expressions of (1) and (4) are no longer applicable. In addition, I_{dlow} in this regime becomes insignificant to circuit performance for its diminishing contribution to I_{deff}. Therefore, high-Vt device data of I_{dlow} at the lowest V_{dd}=0.6V will be excluded from further analysis.

The six types of devices (low-, regular- and high-Vt with two polarities) exhibit interesting I_{dlow} trends in comparison. For example, the I_{dlow}/I_{dsat}-X correlations of all triple-Vt NMOS devices are overlaid onto one another in Figure 4, where regular-Vt and low-Vt devices are virtually on top of each other. High-Vt devices, however, while agreeing closely with the other two devices in the lower- and mid-portions of the correlation curve, show smaller I_{dlow}/I_{dsat} ratios at large X's (approximately for V_{dd} of 1V and above). The same observation equally holds for all PMOS devices, as illustrated in Figure 5. Meanwhile, when all NMOS and PMOS data are overlaid onto each other, a parallel shift is clearly seen with the NMOS' I_{dlow}/I_{dsat} ratio being consistently higher than PMOS' (for both low- and regular-Vt in Figure 6 and high-Vt in Figure 7, respectively).

To explain the above observations, physical mechanisms that discriminate I_{dlow} against I_{dsat} or vice versa in PD SOI devices can be explored. One of these mechanisms is the self-heating effect [5], where the local channel heating results in significantly higher device temperature than the ambient one, leading to drive current degradation. The current degradation (expressed in percentage) dramatically increases with the overall power consumption (i.e., the drain voltage times the current), and is much more pronounced at the I_{dsat} level than at the I_{dlow} level. Consequently, for two devices with the same I_{dlow}/I_{dsat} ratio in the self-heating free environment, I_{dsat} of the device with higher current level incurs more degradation when self-heating takes place, ending up with a higher I_{dlow}/I_{dsat} ratio. Such a mechanism seems to reasonably well explain the difference seen between low-/regular-Vt and high-Vt devices (Figure 4 & Figure 5), where the low- and regular-Vt devices have marginally different current levels, but both significantly higher than those of high-Vt devices. In regions where self-heating is negligible all three devices merge into one characteristic curve. As an indirect proof, the model-simulated I_{dlow}/I_{dsat} ratio is plotted against X with and without the self-heating option turned-on [6], as shown in Figure 8. The relative position of the two curves in Figure 8 rather closely resembles those in Figure 4 & Figure 5. A more direct and definitive proof may be feasible through self-heating free measurement [7].

Another physical mechanism possibly involved is the impact-ionization effect that may noticeably increase the drain current. Particularly for PD SOI devices, the impact

ionization also creates significant accumulation of holes (for NMOS) in the isolated body, and the elevated body voltage further increases the drain current through reduced threshold voltage, known as the kink effect. The I_{dlow} bias conditions coincide with the most favorable conditions for impact ionization [5], subjecting I_{dlow} to its strong influence. I_{dsat}, on the other hand, is under conditions where impact ionization is suppressed because of reduced longitudinal field strength toward the drain end of the channel. The difference in I_{dlow}/I_{dsat} behavior seen between N and P devices (Figure 6 & Figure 7) may be attributed to different impact-ionization behavior of electrons and holes, respectively [8].

Applied to the electrical-test data of an enhanced 90nm technology with embedded SiGe (similar to what is reported in [9]), the proposed I_{dlow} analysis methodology yields a clean correlation curve as in the case of earlier 90nm technologies (Figure 9). A slight tilting change, however, exists between technologies with and without embedded SiGe.

The new I_{dlow} correlation model can be used to generate and check V_{dd} and gate length dependences of I_{dlow} for both target projection and speculative modeling. An example of applying the model to target iteration is shown in Figure 10, where the targets were found to deviate unexpectedly from the latest available electrical-test data at high V_{dd}, and were subsequently revised. A key feature observed in all I_{dlow}/I_{dsat} vs. X correlation curves is their very tight distribution, notwithstanding a wide range of gate length included. Exploiting this feature, I_{dlow} targets of various gate length devices can be effectively screened for them to fall into a tight distribution, as electrical-test data does.

4 CONCLUSIONS

A holistic approach for I_{dlow} analysis has been proposed by taking advantage of its intimate relationships with the ON current, saturation threshold voltage, and supply voltage. The new methodology enables a comprehensive I_{dlow} analysis over a wide range of gate length and supply voltage, as demonstrated on electrical-test data of 90nm multi-Vt PD SOI technologies. Physical mechanisms such as self-heating and impact ionization are offered to explain cross-Vt and cross-polarity I_{dlow} behavior. With the insight and ease of use it offers, the proposed methodology provides practical and efficient guidelines to device target projection and speculative model extraction.

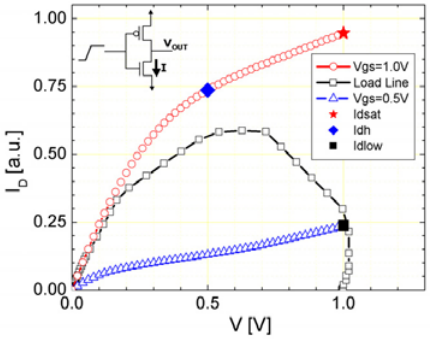

Figure 1 Illustration of I_{dsat}, I_{dh}, and I_{dlow} on example of 1V supply voltage.

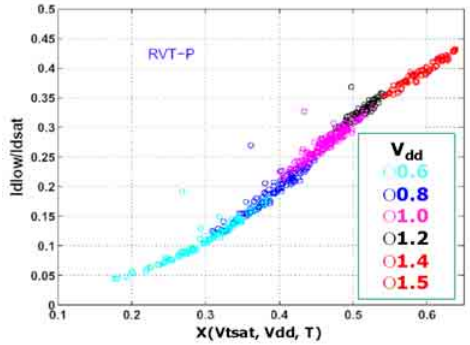

Figure 2 I_{dlow}/I_{dsat} as a function of X for regular-Vt PMOS. The constant-current method is used for V_{tsat} extraction.

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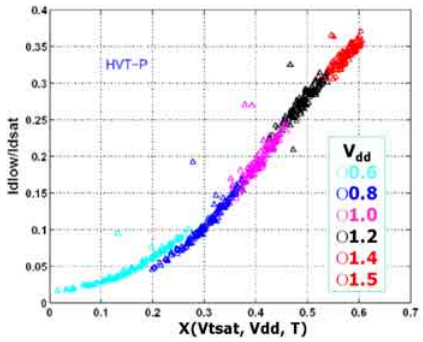

Figure 3 Illustration of deviating trends in high-Vt devices at very low supply voltage (0.6V).

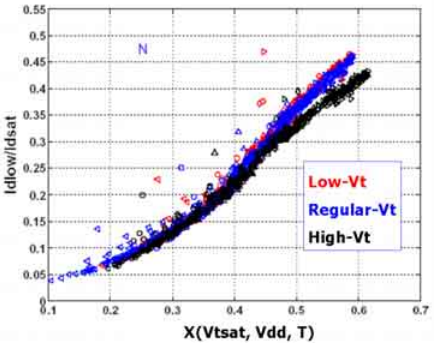

Figure 4 Cross-Vt trend comparison for NMOS.

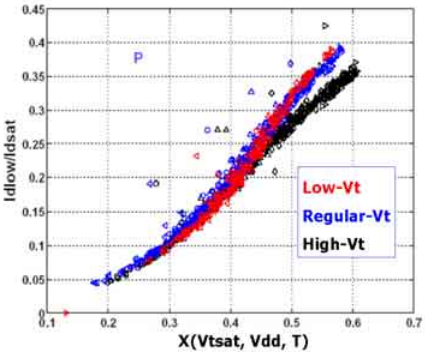

Figure 5 Cross-Vt trend comparison for PMOS.

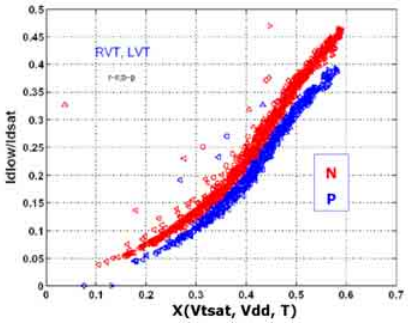

Figure 6 Cross-polarity trend comparison for regular-Vt and low-Vt devices.

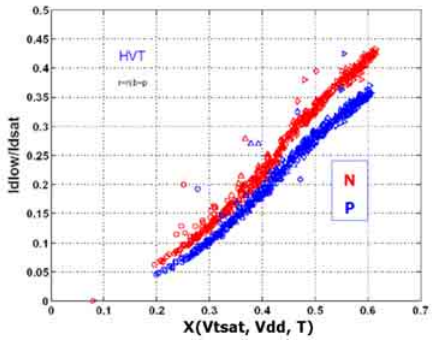

Figure 7 Cross-polarity trend comparison for high-Vt devices.

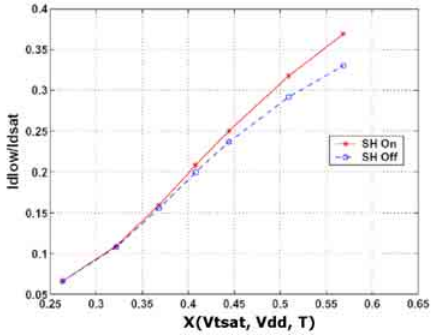

Figure 8 Model-simulated effect of self-heating.

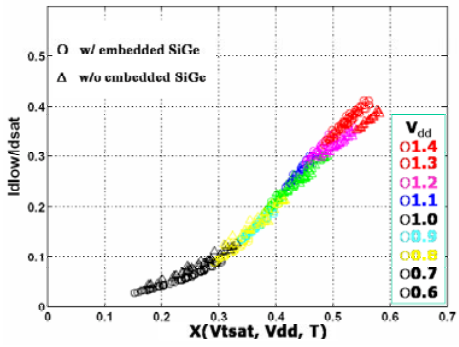

Figure 9 Cross-technology trend comparison: 90nm PD SOI technologies w/ and w/o embedded SiGe.

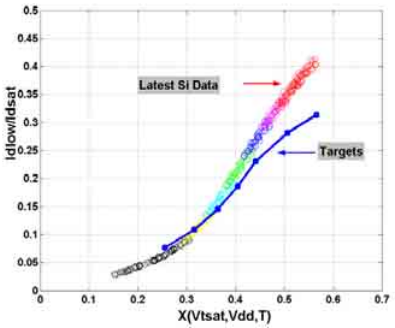

Figure 10 Example of target iteration based on the latest available silicon measurement data.