## EEE598D Homework#5 Instructor: Dr. Hongjiang Song

Fuding Ge, ASU EAST

## Problem 1 A second-order active RC filter building block (or biquad) is shown in Fig. 1.

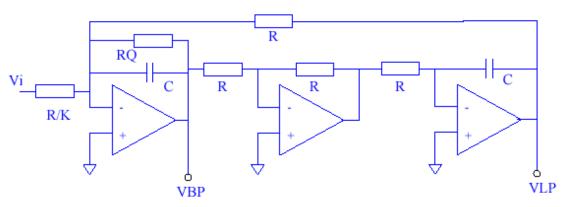
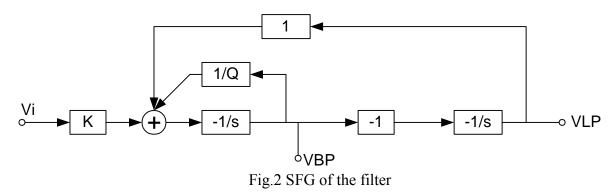


Fig.1 Active RC biquad

**a**): Draw a SFG of this filter.



**b):** Derive the s-domain transfer function (VBP/Vi) and (VLP/Vi) from the SFG. From the SFG we can find that

$$VLP = \frac{1}{s}VBP \tag{1}$$

Or:

$$VBP = sVLP \tag{2}$$

We have:

$$VLP = KVi(-\frac{1}{s^2}) + \frac{sVLP}{Q}(-\frac{1}{s^2}) + VLP(-\frac{1}{s^2})$$
(3)

$$VLPs^{2} = -KVi - \frac{sVLP}{Q} - VLP$$
<sup>(4)</sup>

$$VLP(s^2 + \frac{s}{Q} + 1) = -KVi$$
<sup>(5)</sup>

$$VLP = \frac{-K}{s^2 + \frac{s}{Q} + 1}Vi$$
(6)

From this equation we can see that it shows a low-pass characteristic. From equation (2) we have:

$$VBP = \frac{-Ks}{s^2 + \frac{s}{Q} + 1}Vi$$
(7)

From this equation we can see that VBP shows band pass characteristic.

**c):** Simulate the filter gain and phase responses (for both VBP and VLP outputs) using SPICE under the following conditions:

- Ideal Opamp (gain = 5000)
- R =200k
- C =20pf
- K = 1
- Q = 10

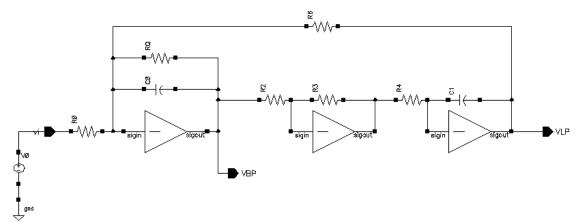


Fig.3 Simulation schematics for the filter

The simulation schematics are shown in Fig.3. The opamp is modeled as a ideal amplifier using VerilogA. Its code is shown below:

```
`include "discipline.h"
`include "constants.h"
module amp(sigin, sigout);
input sigin;
output sigout;
electrical sigin, sigout;
parameter real gain = -5000;
parameter real sigin_offset = 0;
    analog
        V(sigout) <+ gain*(V(sigin) - sigin_offset);
endmodule</pre>
```

The filter is a so-called Tow-Thomas biquad. For a general model, we have [1]:

$$\omega_0^2 = \frac{1}{R_6 R_4 C_0 C_1} \tag{8}$$

$$Q = \frac{R_Q}{R_6 R_4} \sqrt{\frac{C_0}{C_1}} \tag{9}$$

$$K = \frac{R_6}{R_0} \tag{10}$$

Where the definition of  $R_0$ ,  $R_0$ ,  $R_2$ ,  $R_4$ ,  $R_6$  and  $C_0$  and  $C_1$  are shown in Fig.3. For this homework,  $R_0=R_2=R_4=R_6=R=200$ Kohms,  $R_Q=2000$ Kohms,  $C_0=C_1=C=20$ pF. Using equation (8) we find that

$$f_0 = \frac{1}{2\pi RC} = 40kHz \tag{11}$$

$$Q = 10 \tag{12}$$

The SPICE simulation results are shown in Fig.4 and Fig.5.

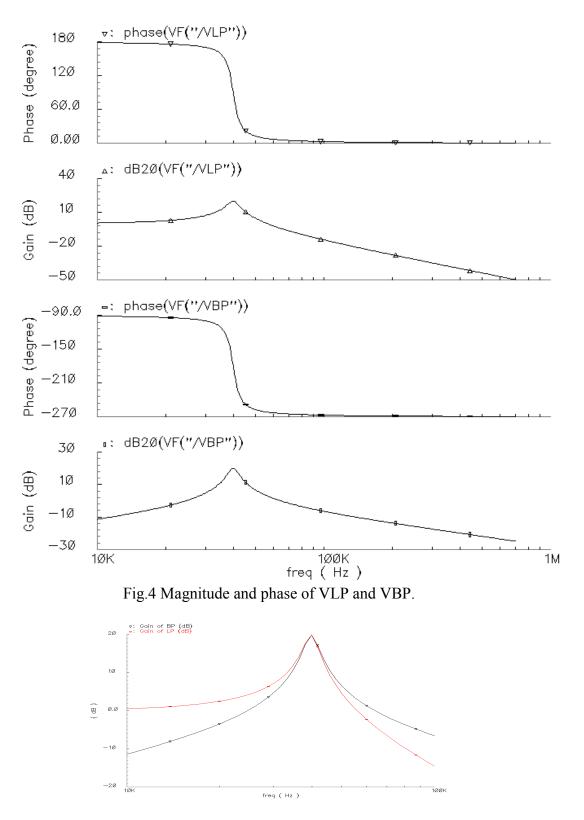


Fig.5 Comparison between the magnitude of VLP and VBP.

The gain of VLP and VBP shows their maximum values at about f=39.81KHz, which is in good agreement with equation (10). The highest value is about 20 dB, which is in agreement with the condition of Q=10. It also can bee seen that at frequency of  $f_0$  VBP and VLP show the same value, which is in agreement with equations (6) and (7). Because Q=10 > 1, VLP shows peak value at about  $f_0$ . Both VLP and VBP are in inversion phase with input (see equation (6) and (7)), so for the low pass signal VLP, its phase at dc is 180 and very high frequency is 0 degree. For the band pass signal, dc phase is -90 degree and very high frequency phase is -270 degree. See Fig.4 for detail.

## Problem 2 A SC circuit realization of the filter shown in Fig.1 is given in Fig. 6.

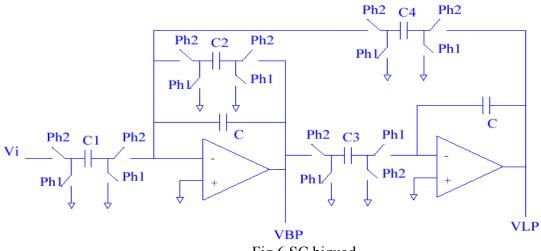


Fig.6 SC biquad

Where ph1 and ph2 are two-phase non-overlap clocks and assume T = 1us

a) Find the value of C, C1, C2, C3, and C4

From Problem 1 we know C=20pF.

From the SC theory we know the equivalent resistance of the switched capacitor is:

$$R = \frac{T}{C} \tag{8}$$

With T=1us and R=200K and K=1, we have

$$C_1 = \frac{T}{KR} = \frac{10^{-6}}{200 \times 10^{-3}} = 5 \times 10^{-12} F = 5 \, pF \tag{9}$$

With Q=10 we have:

$$C_2 = \frac{T}{QR} = \frac{10^{-6}}{10 \times 200 \times 10^{-3}} = 0.5 \times 10^{-12} F = 0.5 \, pF \tag{10}$$

$$C_3 = C_4 = C_1 = 5\,pF \tag{11}$$

**b**): Simulate the frequency responses (both VBP and VLP output) of this SC filter using SWITCAP and compare you results with results from problem1.

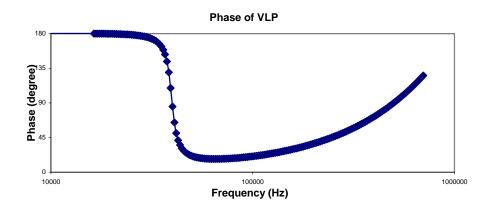


Fig.7 Phase of low pass signal

Compare this figure with Fig.4 we find that for this SC circuit, the phase never reaches 0 while for the CT filter at very high frequency the phase is about 0 degree. The lowest point of the phase, about 17.5 degree, occurs at frequency of 65.4 KHz for the SC circuit. At the frequency of 39.8KHz, where the CT circuit shows peak gain and a phase of 90 degree, the SC shows a phase about 86 degree.

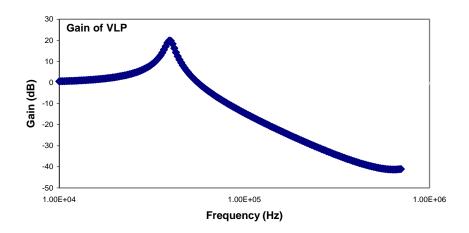


Fig.8 Gain of low pass signal

For the SC circuit, peak gain is about 19.94 dB at a frequency of 39.2KHz. This value is quite close to CT circuits. At 50 KHz, which is half of the sampling frequency, the gain of SC is about 3.83 dB while the CT shows a gain of 3.9dB, still quite close to each other. But at high frequency, the SC circuit shows less attenuation than CT circuit. For example at 700 KHz, the gain of SC is about -41 dB while the CT shows a gain of 50 dB.

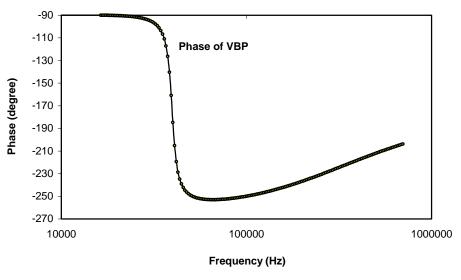


Fig.9 Phase of band pass signal

For the band pass signal, the lowest phase of SC is about -250. Then it goes up. For the CT circuit at high frequency the phase reaches a value of about -270 degree.

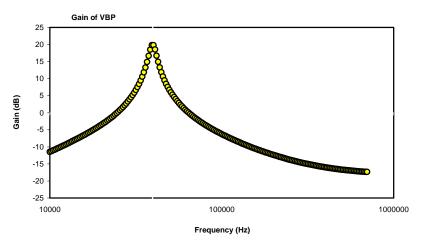


Fig.10 Gain of band pass signal

For the gain of the band pass signal, the peak values of the CT and SC are quite close, around 19.8 dB. At higher frequency the gain of SC shows less attenuation than that of CT circuit.

c) Show your SWITCAP simulation setup (Netlist, analysis, plot/print etc.)

timing: period 1e-6; clock clk 1 (0 1/2); end; sil (2 0) clk; sil (1 0) clk; sil (1 0) clk; sil (1 0) clk; sil (2 0) clk; cl (2 3) 5e-12; cl (1 2 3) 5e-13; cl (2 3) 5e-12; cl (1 0) field; sil (2 0) cl (2 0) clk; cl (2 3) 5e-12; cl (1 0) field; cl (2 3) 5e-12; cl (1 0) field; cl (2 3) 5e-12; cl (1 0) field; sil (2 0) cl (2 0) c	
clock clk 1 (0 1/2); end; s11 (2 0) clk; s12 (3 0) clk; s13 (12 0) clk; s14 (13 0) clk; s16 (11 0) clk; s16 (11 0) clk; s17 (6 0) clk; s21 (1 2) #clk; s22 (3 4) #clk; s23 (4 12) #clk; s23 (4 12) #clk; s23 (4 12) #clk; s25 (4 10) #clk; s26 (11 9) #clk; s27 (5 6) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; vi (1 0); end; analyze ss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(6); plot vdb(9) vp(9); plot vdb(9) vdb(9) vdb(9) vdb(9) vdb(9) vdb(9) vdb(9) vdb(9) vdb(9) vd	timing;
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<pre>s11 (2 0) clk; s12 (3 0) clk; s13 (12 0) clk; s14 (13 0) clk; s15 (10 0) clk; s16 (11 0) clk; s17 (6 0) clk; s18 (7 8) clk; s22 (3 4) #clk; s22 (3 4) #clk; s22 (3 4) #clk; s23 (4 12) #clk; s24 (13 5) #clk; s25 (4 10) #clk; s26 (1 10) #clk; s27 (5 6) #clk; s28 (7 0) #clk; s29 (2 12 3) 5e-12; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; c6 (8 9) 20e-12; c7 (1 (5 0 0 4) 5000; e1 (1 0); end; analyze sss; set via c 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); print vdb(5) vp(5);</pre>	
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<pre>s13 (12 0) elk; s14 (13 0) elk; s15 (10 0) elk; s17 (6 0) elk; s18 (7 8) elk; s21 (1 2) #elk; s22 (3 4) #elk; s23 (4 12) #elk; s24 (13 5) #elk; s25 (4 10) #elk; s25 (4 10) #elk; s25 (4 10) #elk; s26 (11 9) #elk; s27 (5 6) #elk; s28 (7 0) #elk; s28 (7 0) #elk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; e1 (1 0); end; analyze ss; set via c1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;</pre>	
<pre>s14 (13 0) clk; s15 (10 0) clk; s16 (1 0) clk; s17 (6 0) clk; s22 (3 4) #clk; s22 (3 4) #clk; s23 (4 12) #clk; s23 (4 12) #clk; s25 (4 10) #clk; s25 (4 10) #clk; s25 (4 10) #clk; s26 (11 9) #clk; s27 (15 6) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;</pre>	
<pre>s15 (10 0) clk; s17 (6 0) clk; s17 (6 0) clk; s18 (7 8) clk; s22 (3 4) #clk; s22 (3 4) #clk; s24 (12) #clk; s23 (4 12) #clk; s24 (13 5) #clk; s24 (13 5) #clk; s25 (4 10) #clk; s25 (4 10) #clk; s27 (5 6) #clk; s28 (7 0) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze ss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(5) vp(6); plot vdb(9) vp(9); end;</pre>	
<pre>s16 (11 0) clk; s17 (6 0) clk; s18 (7 8) clk; s22 (3 4) #clk; s22 (3 4) #clk; s23 (4 12) #clk; s24 (13 5) #clk; s25 (4 10) #clk; s26 (11 9) #clk; s27 (5 6) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze ss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;</pre>	
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<pre>s23 (4 12) #clk; s24 (13 5) #clk; s25 (4 10) #clk; s26 (11 9) #clk; s27 (5 6) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(9) vp(9); end;</pre>	
<pre>\$24(135) #clk; \$25(410) #clk; \$27(56) #clk; \$27(56) #clk; \$28(70) #clk; c1 (23)5e-12; c2 (1213)5e-13; c3 (67)5e-12; c4 (1011)5e-12; c5 (45)20e-12; c6 (89)20e-12; e1 (5 0 0 4)5000; e2 (9 0 0 8)5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;</pre>	
s25 (4 10) #clk; s26 (11 9) #clk; s27 (5 6) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); plot vdb(9) vp(9); end;	
<pre>s26 (11 9) #clk; s27 (5 6) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); plot vdb(9) vp(9); end;</pre>	
s27 (5 6) #clk; s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end; end;	
s28 (7 0) #clk; c1 (2 3) 5e-12; c2 (12 13) 5e-13; c3 (6 7) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); plot vdb(9) vp(9); end;	
c1 (23) 5e-12; c2 (1213) 5e-13; c3 (67) 5e-12; c4 (1011) 5e-12; c5 (45) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;	
c2 (12 13) 5e-13; c3 (67) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); end;	SZS(70) #CIR;
c2 (12 13) 5e-13; c3 (67) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); end;	
c3 (67) 5e-12; c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); end; end;	
c4 (10 11) 5e-12; c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); end;	
c5 (4 5) 20e-12; c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;	
c6 (8 9) 20e-12; e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); plot vdb(9) vp(9); end;	
e1 (5 0 0 4) 5000; e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); end;	
e2 (9 0 0 8) 5000; vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); end;	c6 (8 9) 20e-12;
vi (1 0); end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	e1 (5 0 0 4) 5000;
end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	e2 (9 0 0 8) 5000;
end; analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	vi (10);
analyze sss; set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	
set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	
set vi ac 1 0; infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	analyze sss:
infreq 10e3 700e3 log 200; print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	
print vdb(5) vp(5); plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	
plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	
plot vdb(5) vp(5); print vdb(9) vp(9); plot vdb(9) vp(9); end;	print vdb(5) vp(5)
print vdb(9) vp(9); plot vdb(9) vp(9); end;	
plot vdb(9) vp(9); end;	
end;	
end;	
	end;

## **Reference:**

[1] R. Schaumann, M.E. Van Valkenburg, "Design of analog filters", Oxford university press, New York, 2001