Spring 2002

EEE598D: Analog Filters & Signal Processing Circuits

Instructor:

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Today: Introduction to SI Circuits

- Basic SI Circuits
- Errors of Practical SI Circuits
- Basic SI Building Blocks

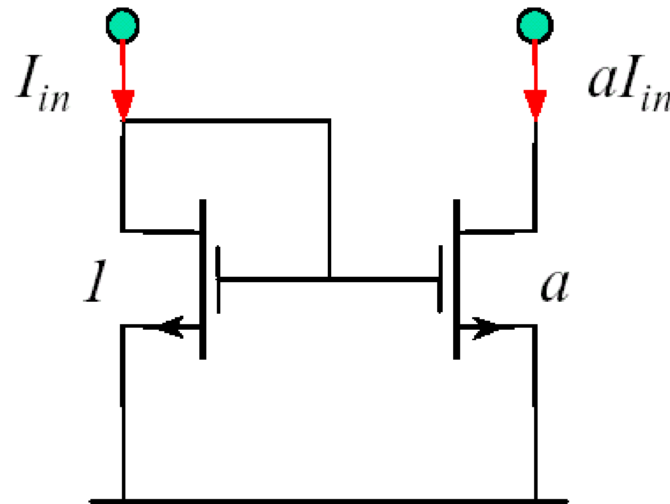
Why SI Technique?

- The switched-current (SI) technique for analog signal processing gained interest because of it ability to adapt to digital VLSI trends.
  - Low supply voltage
  - Poor device linearity
  - Lack of precision analog devices
  - Potentially high-speed
  - Very regular structure
- In SI circuits, signal is represented as CURRENT.
  - Imply no DIRECT impact of voltage scaling to signal swing

SI or SC Circuits?

- Switched-current
  - low-voltage supply
  - high-speed
  - non-linear capacitors
  - no operational amps
  - modularity
  - possible to increase DR while keeping speed
  - 0.1% matching
- Switched-capacitor
  - high-accuracy
  - linear capacitors
  - high dynamic range
  - stability problems (opamps)
  - Different loads -> diff. OP architectures
  - 0.01% matching

Basic CMOS Current Mirror



$$\frac{I_{out}}{I_{in}} = \frac{\mu_0 C_{ox}}{\mu_0 C_{ox}} \frac{aW/L}{W/L} \frac{(V_{in} - V_{T2})^2}{(V_{in} - V_{T1})^2} \frac{1+\lambda_2 V_{out}}{1+\lambda_1 V_{in}} \approx \frac{a \cdot I_{in}}{I_{in}} \approx a$$

SI Circuit Principle

- The current through the transistor can be held using a capacitor storing the gate-source voltage of the transistor.

The First-Generation Memory Cell

I aI

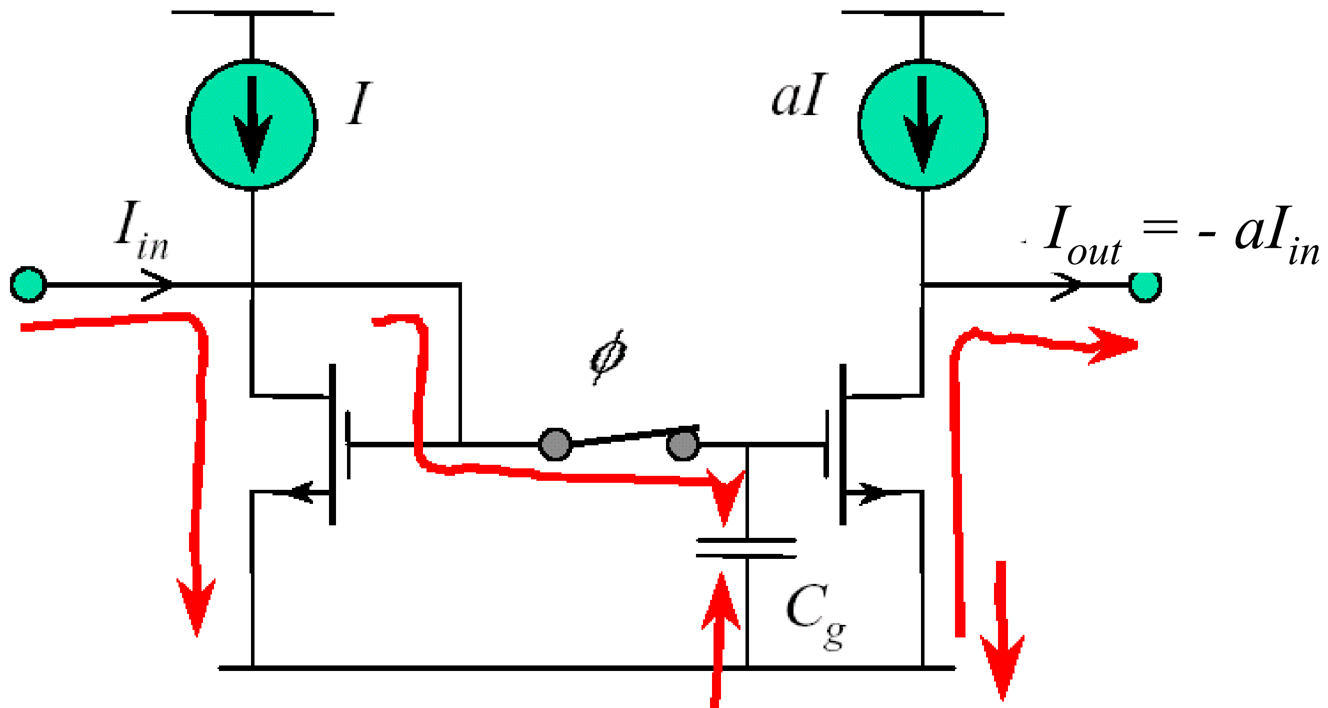
I_{in} I_{out}

ϕ

C_g

The First-Generation Memory Cell

- Phase 1



The First-Generation Memory Cell

- Phase 2

I

aI

I_{in}

$I_{out} = -aI_{in}$

ϕ

C_g

V_{gs} is maintained!

SI Output Signal Waveform

First generation current memory cell

Io

Iin

Amplitude

time

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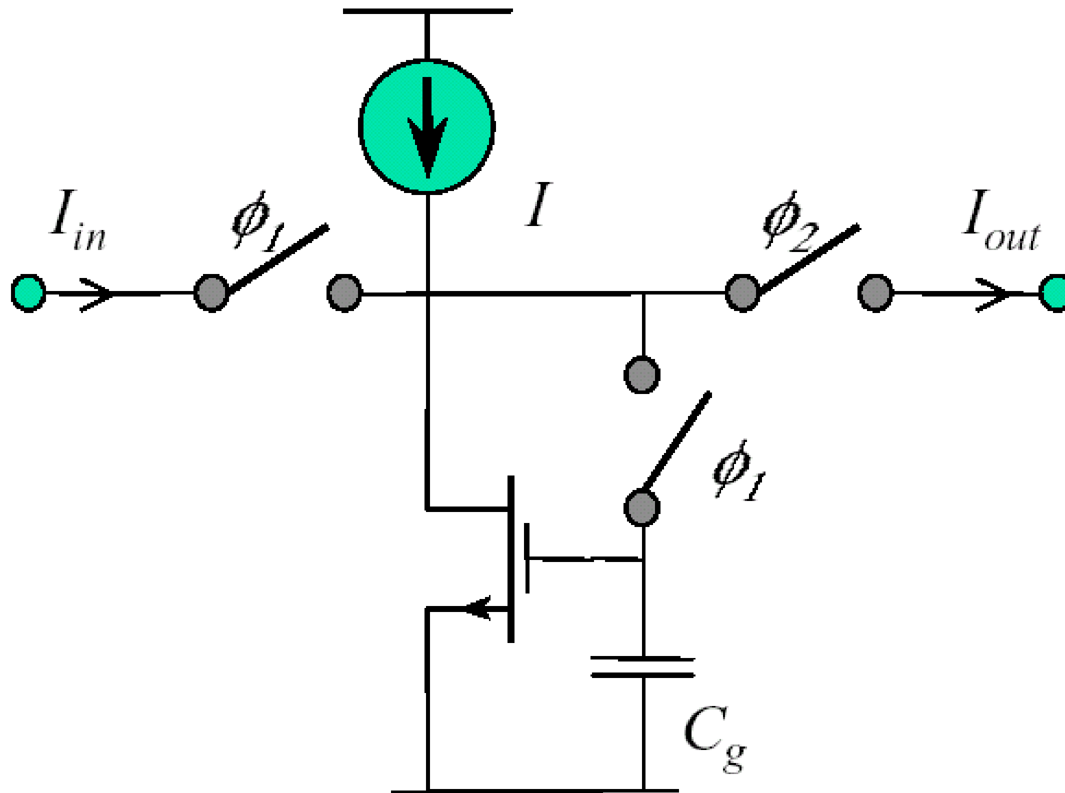
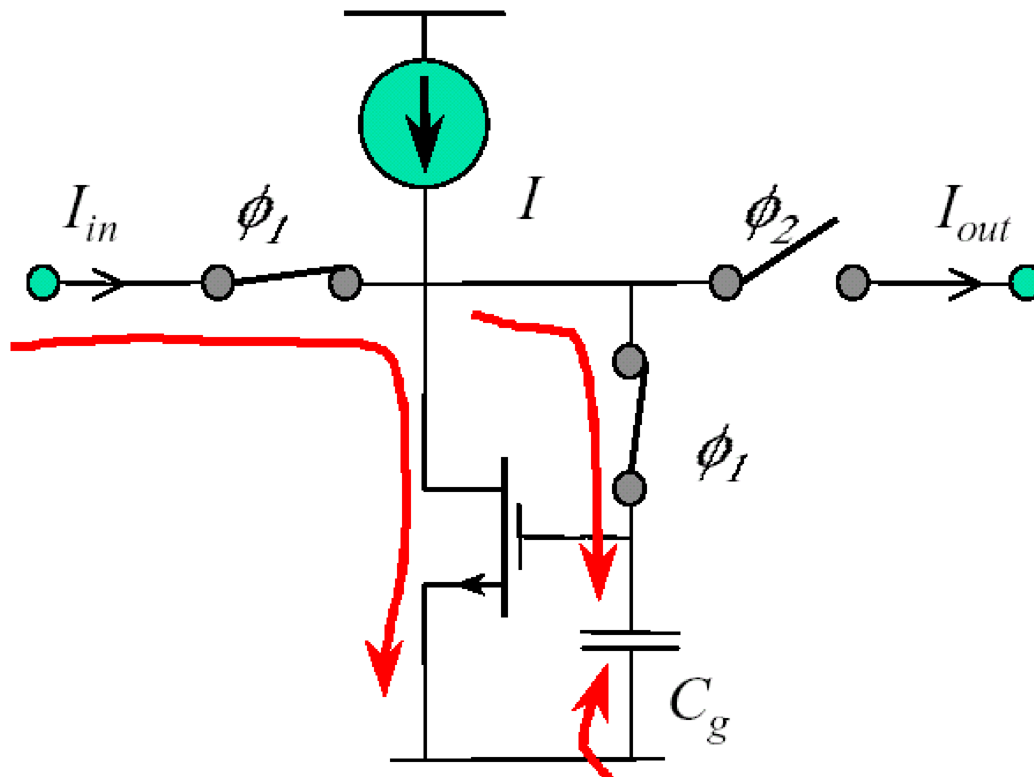
The Second-Generation Memory Cell



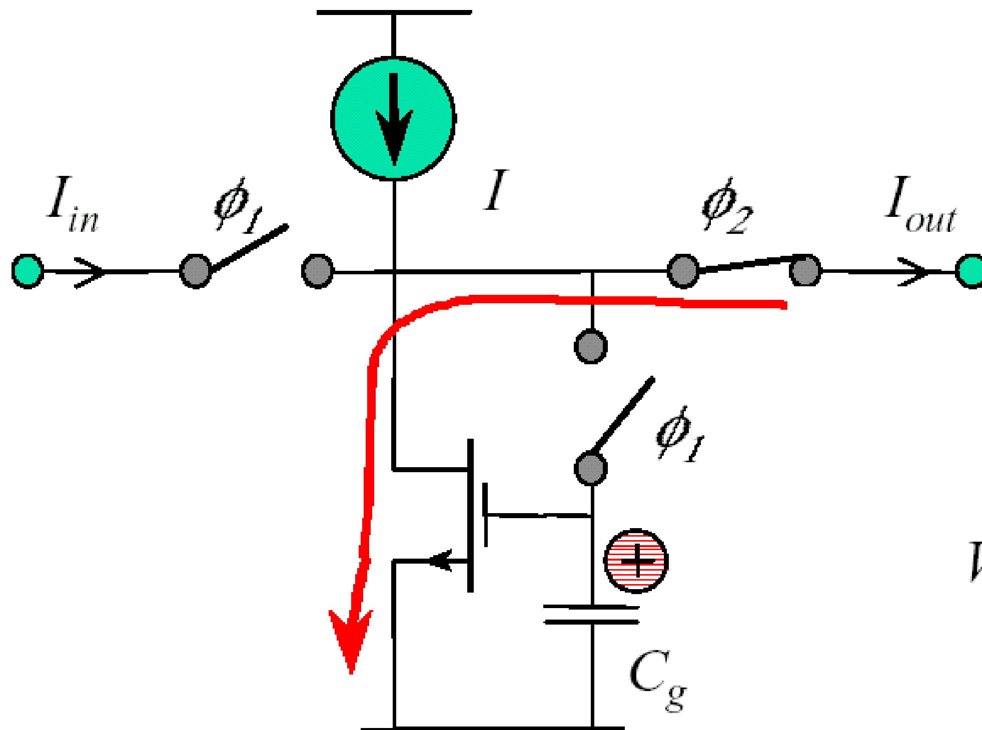
The Second-Generation Memory Cell

- Phase 1



The Second-Generation Memory Cell

- Phase 2



V_{gs} is maintained!

Comparison

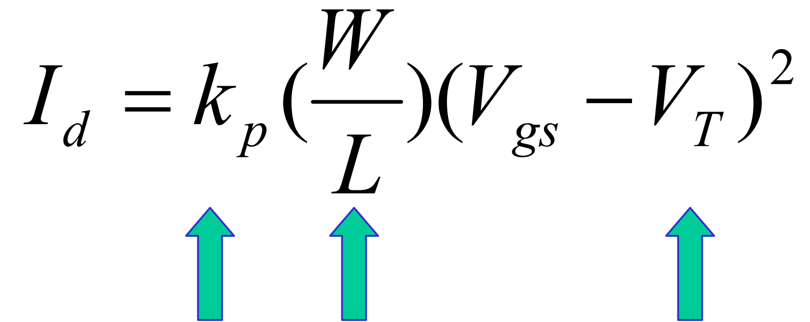
- First generation
  - Matching sensitive
  - Simple switching
  - High fan out
- Second generation
  - Matching insensitive
  - Low fan out
  - Less area
  - 1/f noise decreased
  - Complex switching

Non-ideal Effects in Practical SI Circuits

- Device mismatches
- Channel length modulation
- Charge Injection
- Noise
- Settling and Leakage
- Power Line drop and bias mismatch
- Clock Jitter

Device Mismatches

- MOS transistor mismatch
  - Doping concentration
  - Oxide thickness
  - Finite edge resolution
  - Lateral diffusion



$$I_d = k_p \left(\frac{W}{L}\right)(V_{gs} - V_T)^2$$

- Causes linear gain and constant offset errors

$$i_{out} = (1+\varepsilon)i_{in} + \varepsilon I$$

Device Mismatches (Con't)

- Global MOS transistor mismatch
  - Absolute mismatch
  - Overall PVT shift of process run
  - Long distance variation
- Local MOS transistor mismatch
  - Relative mismatch
  - PVT variation of nearby devices

Device Mismatch Minimization

- Device size/area
- Device separation
- Bias current

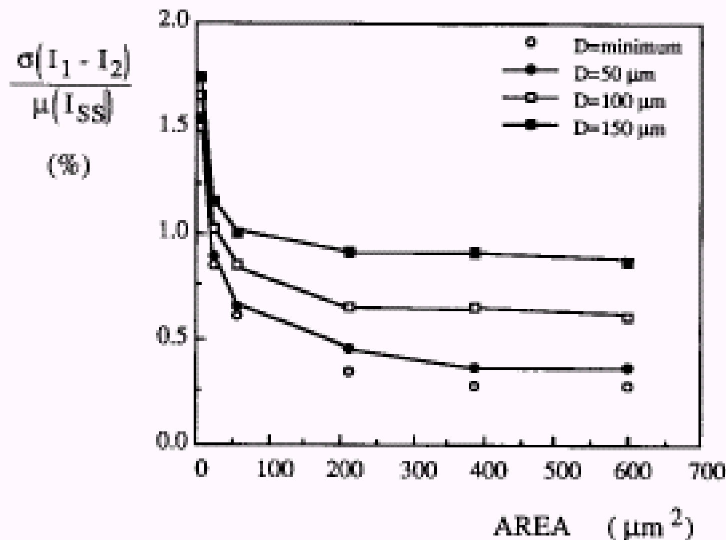


Fig. 13. Simulated device area and separation distance dependence of current mirror circuit. All simulations performed at $I_{SS} = 50\ \mu A$ and $W/L = 1.5$.

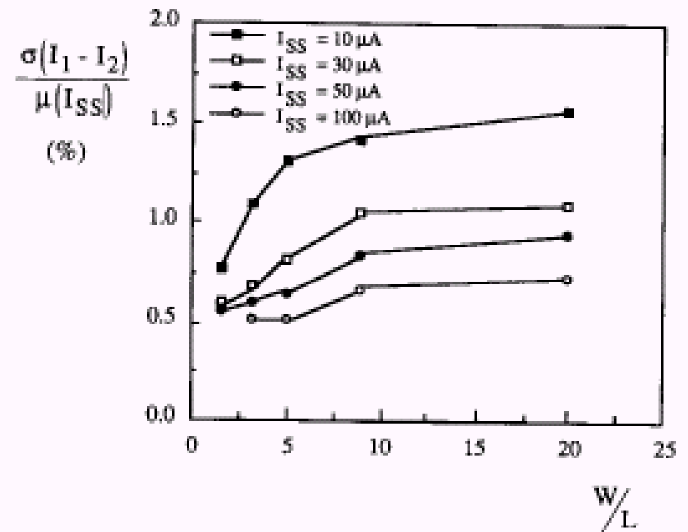
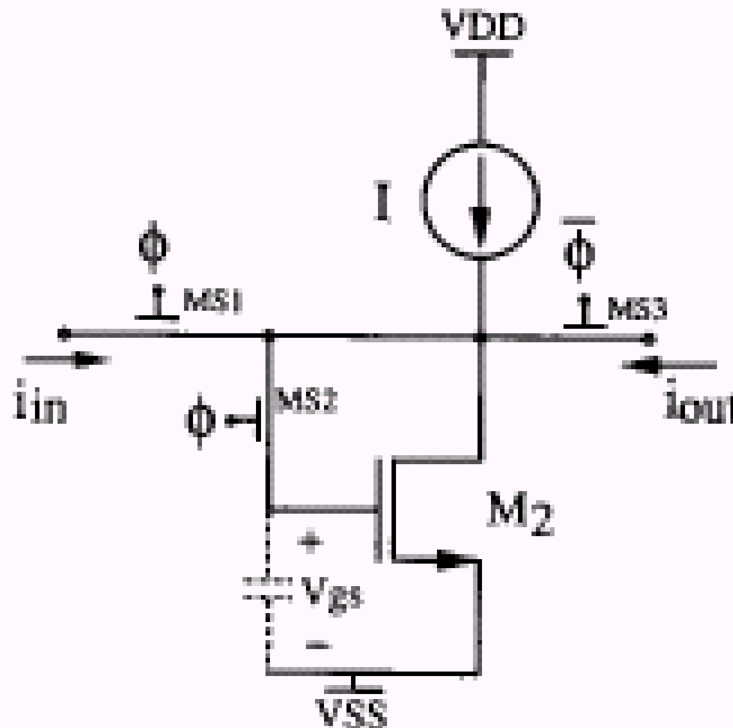


Fig. 14. Simulated bias dependence of current mirror circuit. All simulations performed for device areas of 80 μm^2 and at minimum separation distances.

C. Michael, et al. IEEE JSSC Vol.27 No.2 Feb., 1992. Pp.154-166

Device Mismatch Minimization

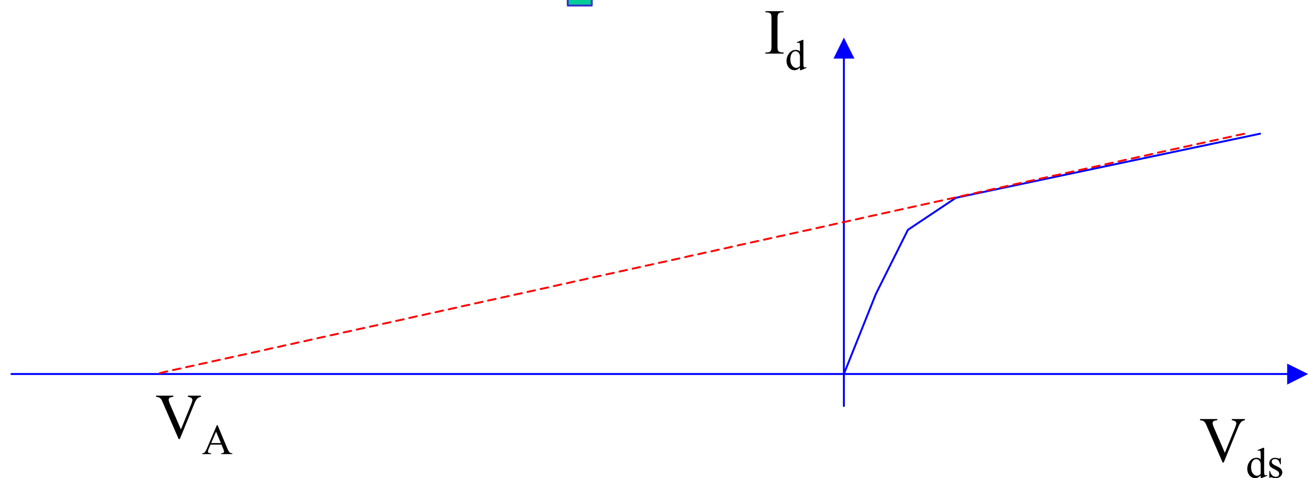
- Dynamic Current Mirror



Channel Length Modulation

- Output resistance
- Early voltage

$$I_d = k_p(\frac{W}{L})(V_{gs} - V_T)^2(1 + \lambda V_{ds})$$



Channel Length Modulation Minimization

- Cascade techniques

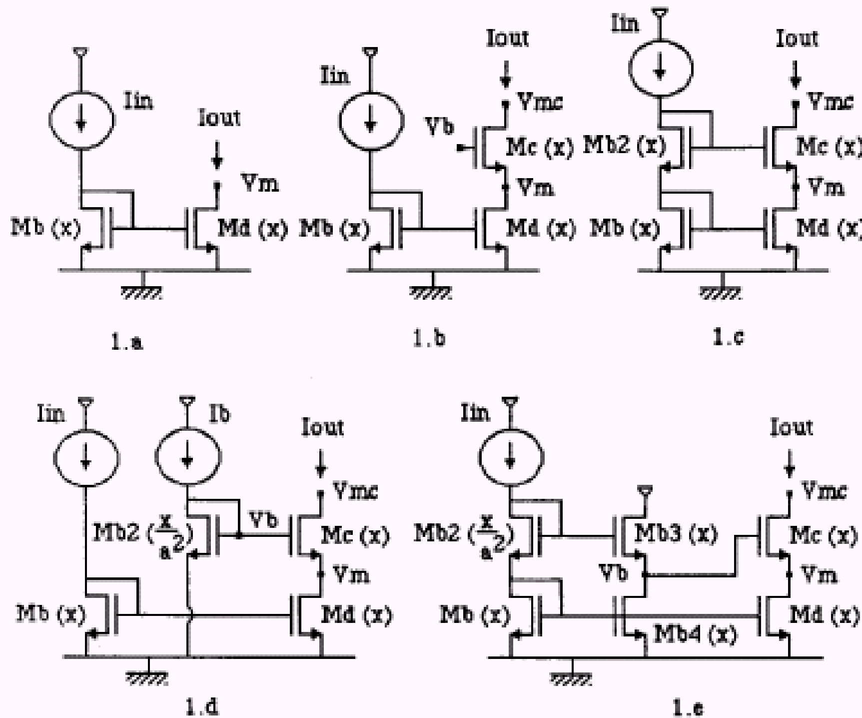


Fig 1. Circuit diagrams of common used current mirror structures (Iin ≤ Ib)

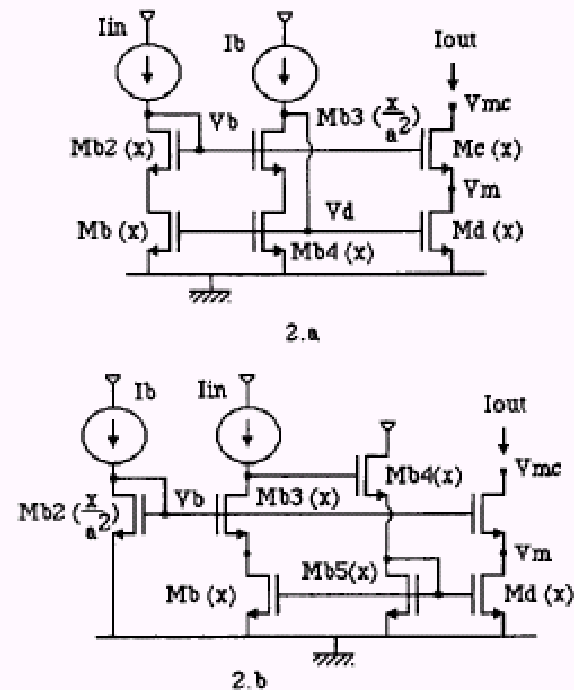
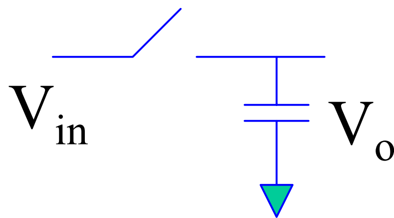
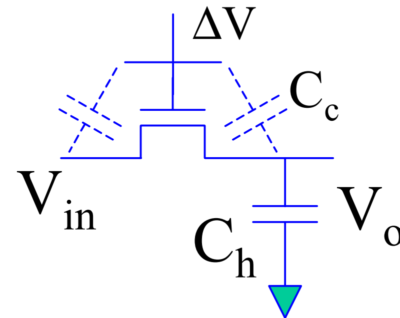


Fig 2. Current mirror structures reducing the channel length modulation

Clock Feed Through (CFT)

- Switch signal coupling to the analog signal through the switches
- Channel-charge injection
- Causes nonlinear gain and constant offset errors



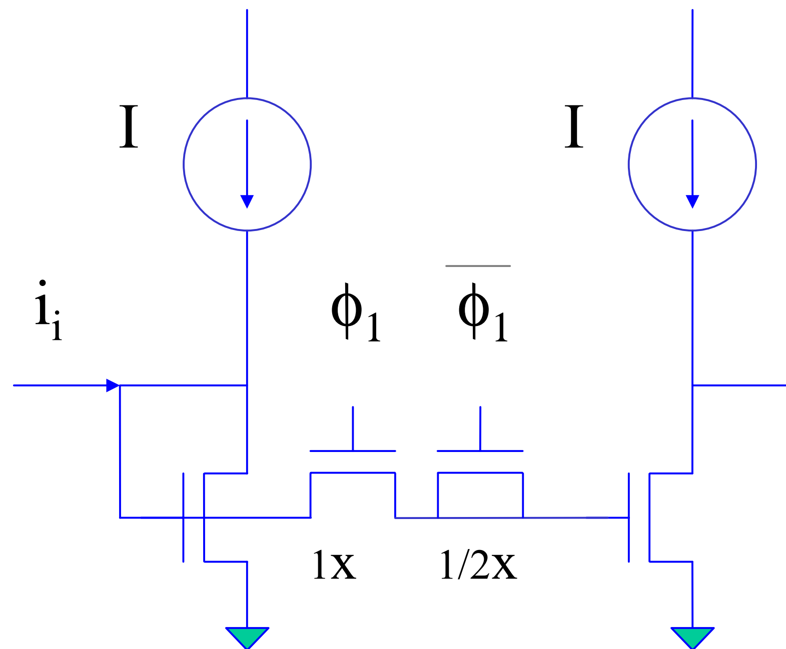


$$V_o = V_{in}$$

$$V_o \approx V_{in} - (C_c / C_h)\Delta V$$

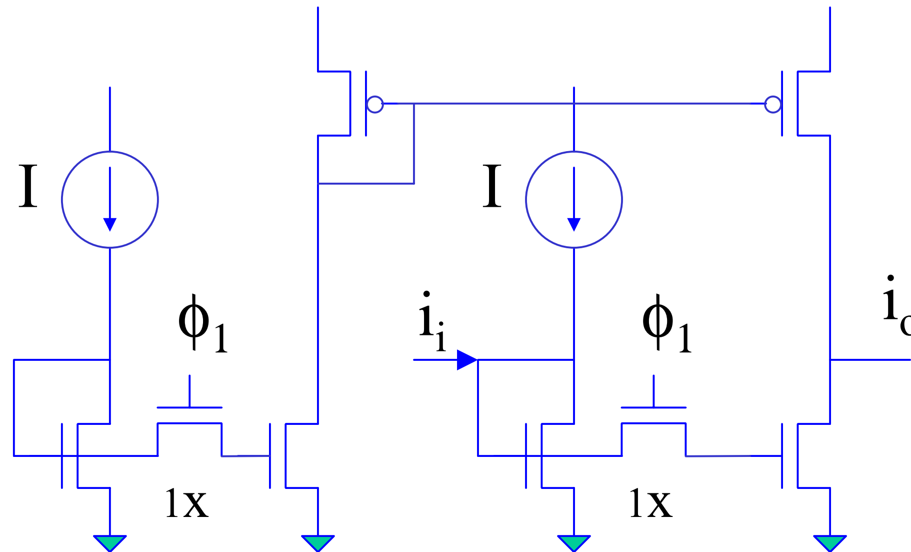
CFT Minimization

- Dummy switch device (I)



CFT Minimization

- Dummy switch device (II)



Noise

- Continuous-Time Circuit Noise
  - Thermal noise
  - Flicker noise
  - Shot noise
- Switching Noise
  - Substrate
  - Power line
  - Cross-cap

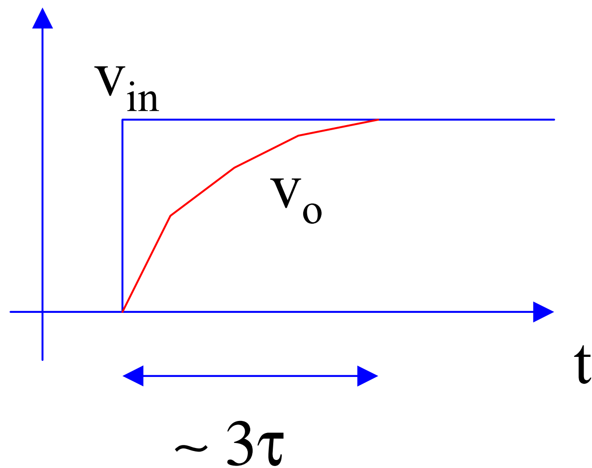
$$S_{thermal} = \frac{8kTg_m}{3}$$

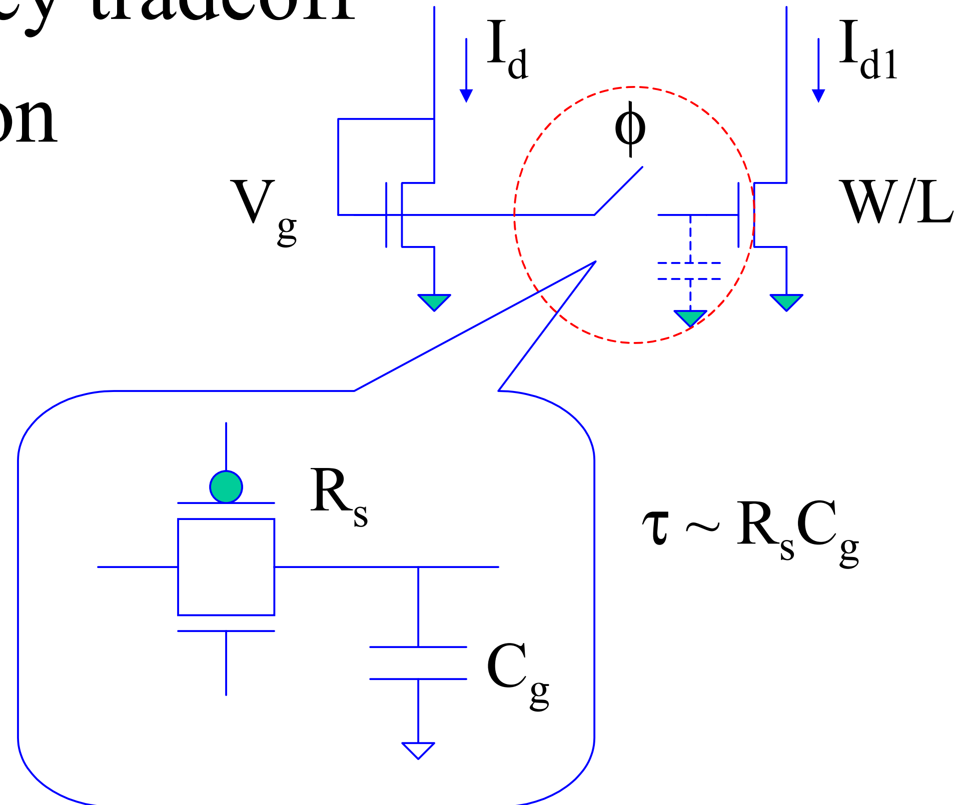
$$S_{flick} = \frac{\alpha}{C_{ox}WL}\frac{1}{f}$$

$$S_{shot} = 2qI_{dj}$$

Settling

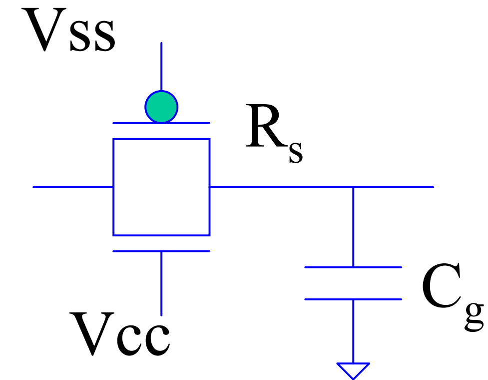
- Speed vs. Accuracy tradeoff
- Low Vcc limitation



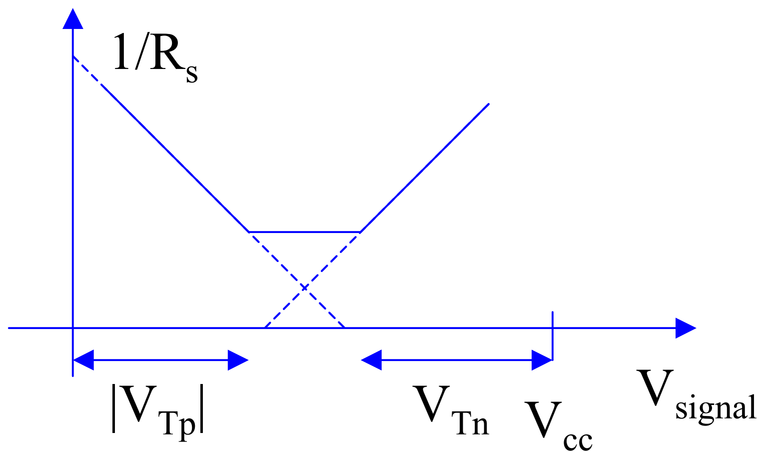


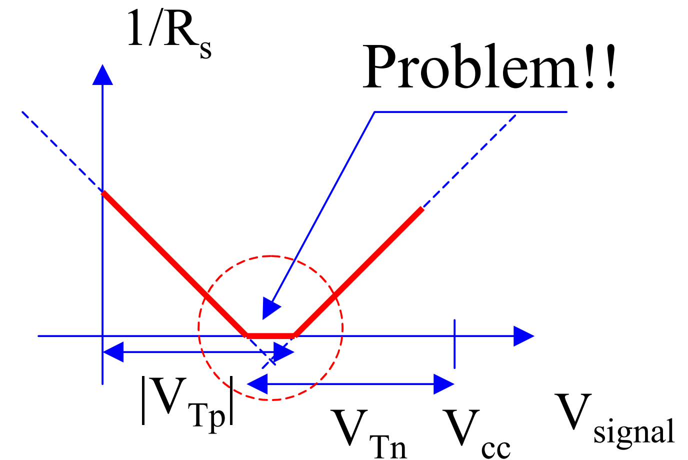
$\tau \sim R_s C_g$

Settling



$$\frac{1}{R_s} \approx \beta_n (V_{cc} - V_{Tn} - V_{signal}) + \beta_p (V_{signal} - |V_{Tp}|)$$



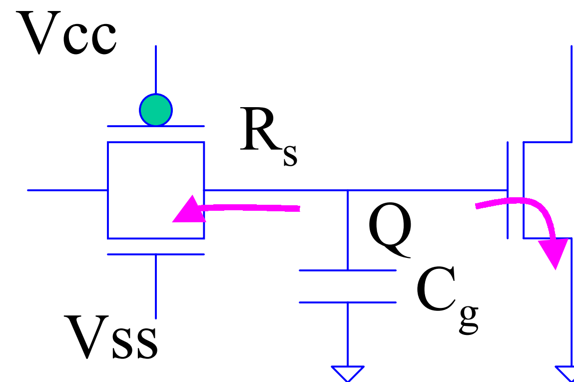


A) $V_{Tn} + |V_{Tp}| < V_{cc}$

B) $V_{Tn} + |V_{Tp}| > V_{cc}$

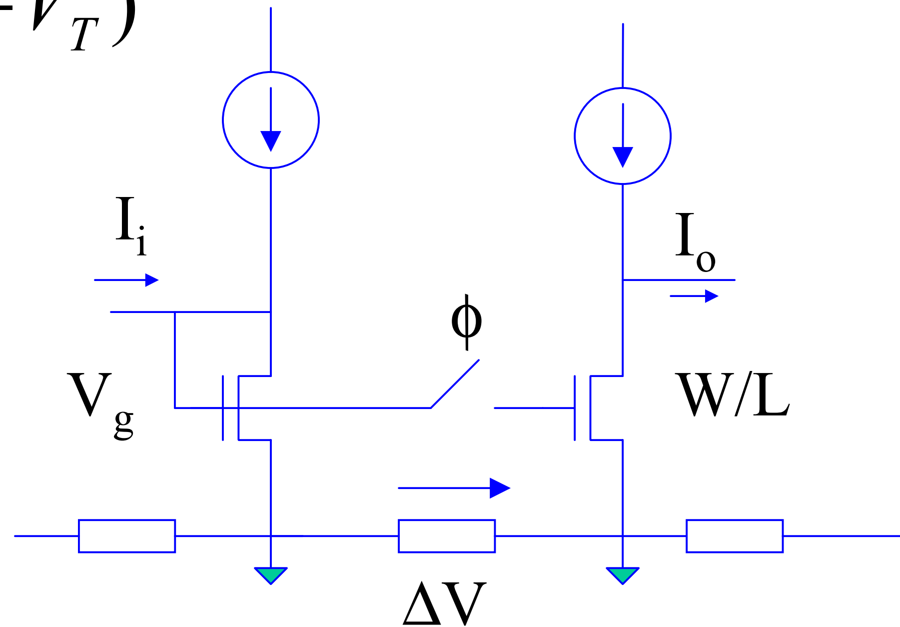
Leakage

- Diode leakage
- Gate leakage
- Low frequency limit



Power Line IR Drop and Bias Mismatch

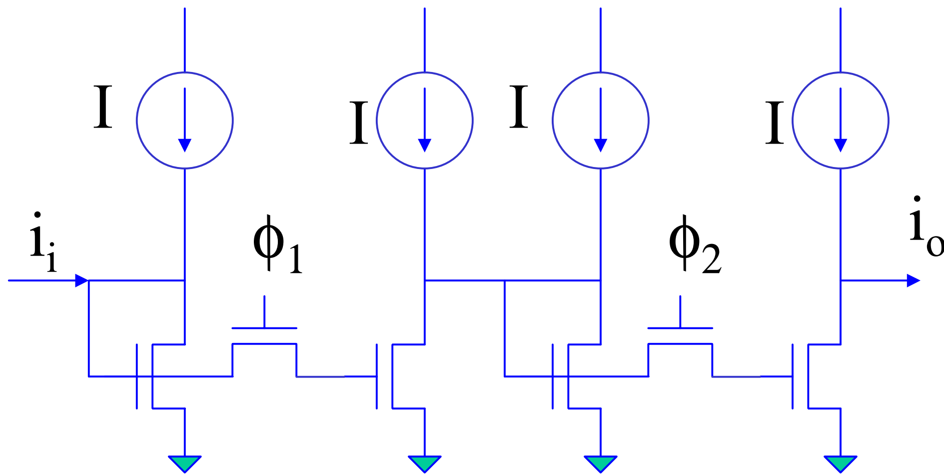
$$\frac{\Delta I_d}{I_d} \approx \frac{2\Delta V_{gs}}{(V_{gs} - V_T)}$$

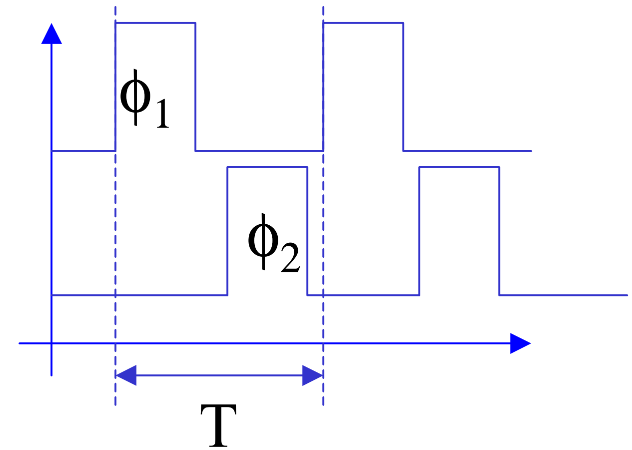


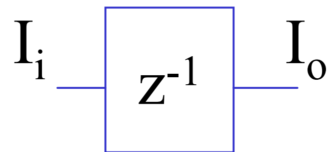
Basic SI Filter Building Blocks

- SI Delay Elements
- SI Adder
- SI Scalar
- SI Integrator

SI Delay Element





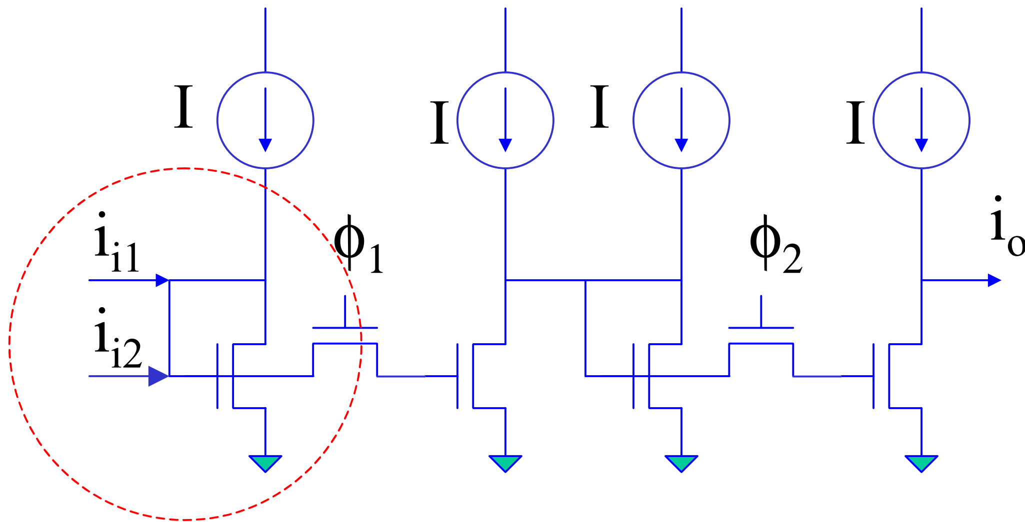


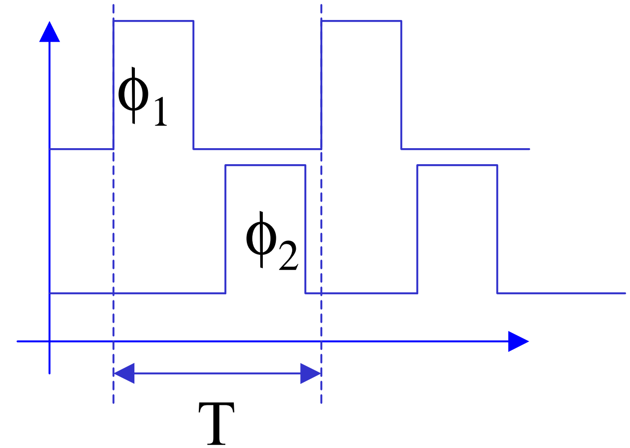
$$i_o(nT) = i_i((n-1)T)$$

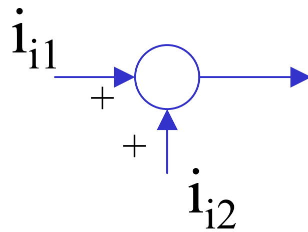
or

$$I_o(z) = z^{-1} I_i(z)$$

SI Adder



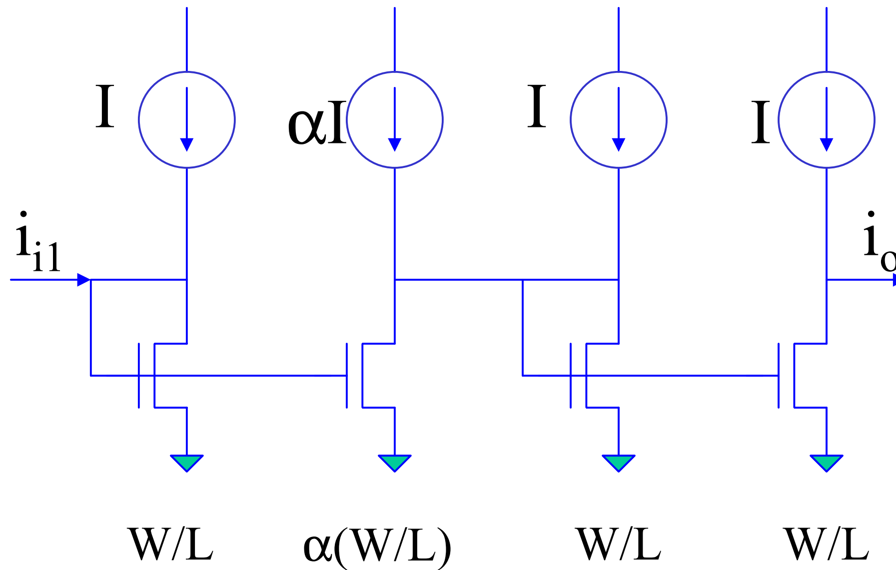


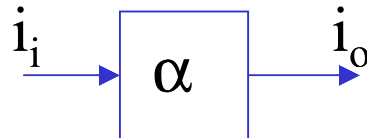


$$i_o(nT) = i_{i1}(nT) + i_{i2}(nT)$$

$$I_o(z) = I_{i1}(z) + I_{i2}(z)$$

SI Scalar



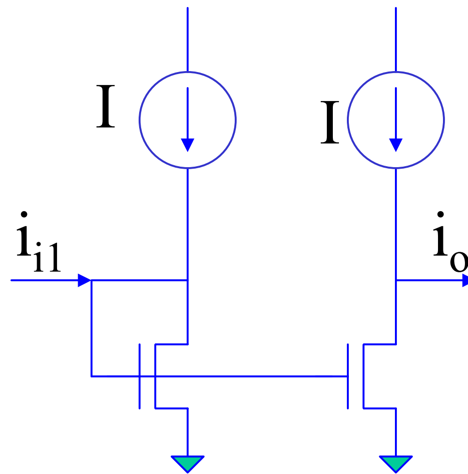


$$i_o(nT) = \alpha i_i(nT)$$

or

$$I_o(z) = \alpha I_i(z)$$

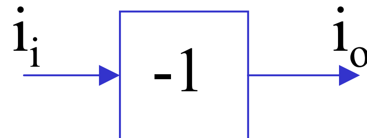
SI Inverter



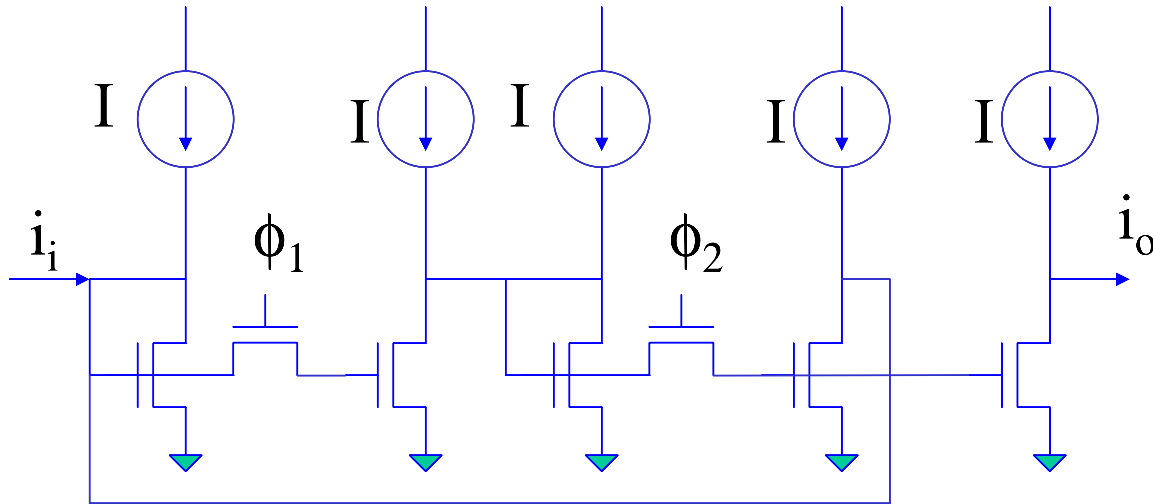
$$i_o(nT) = -i_i(nT)$$

or

$$I_o(z) = -I_i(z)$$



SI Integrator



$$i_o(nT) = i_o((n-1)T) + i_i((n-1)T)$$

or

$$\frac{I_o(z)}{I_i(z)} = \frac{z^{-1}}{1-z^{-1}}$$