Spring 2002

EEE598D: Analog Filters & Signal Processing Circuits

Instructor:
Dr. Hongjiang Song

Department of Electrical Engineering
Arizona State University

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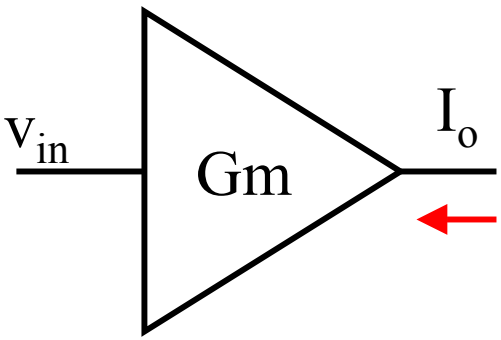
Today: Introduction to Gm-C Circuits (I)

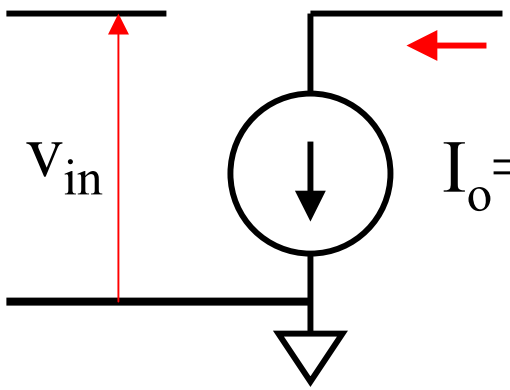
- Basic building blocks of Gm-C filters
- MOS linear transconductor realization techniques

Basic Building Block of Gm-C filters

- Transconductor



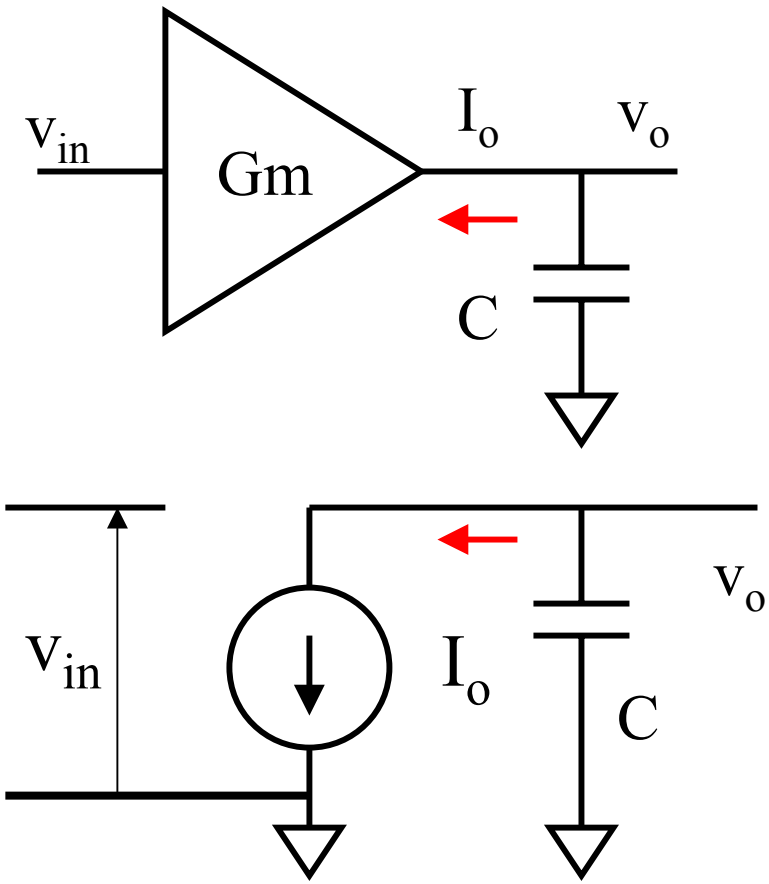
$$i_o = g_m v_{in}$$



I_o= Gm Vin

Basic Building Block of Gm-C filters

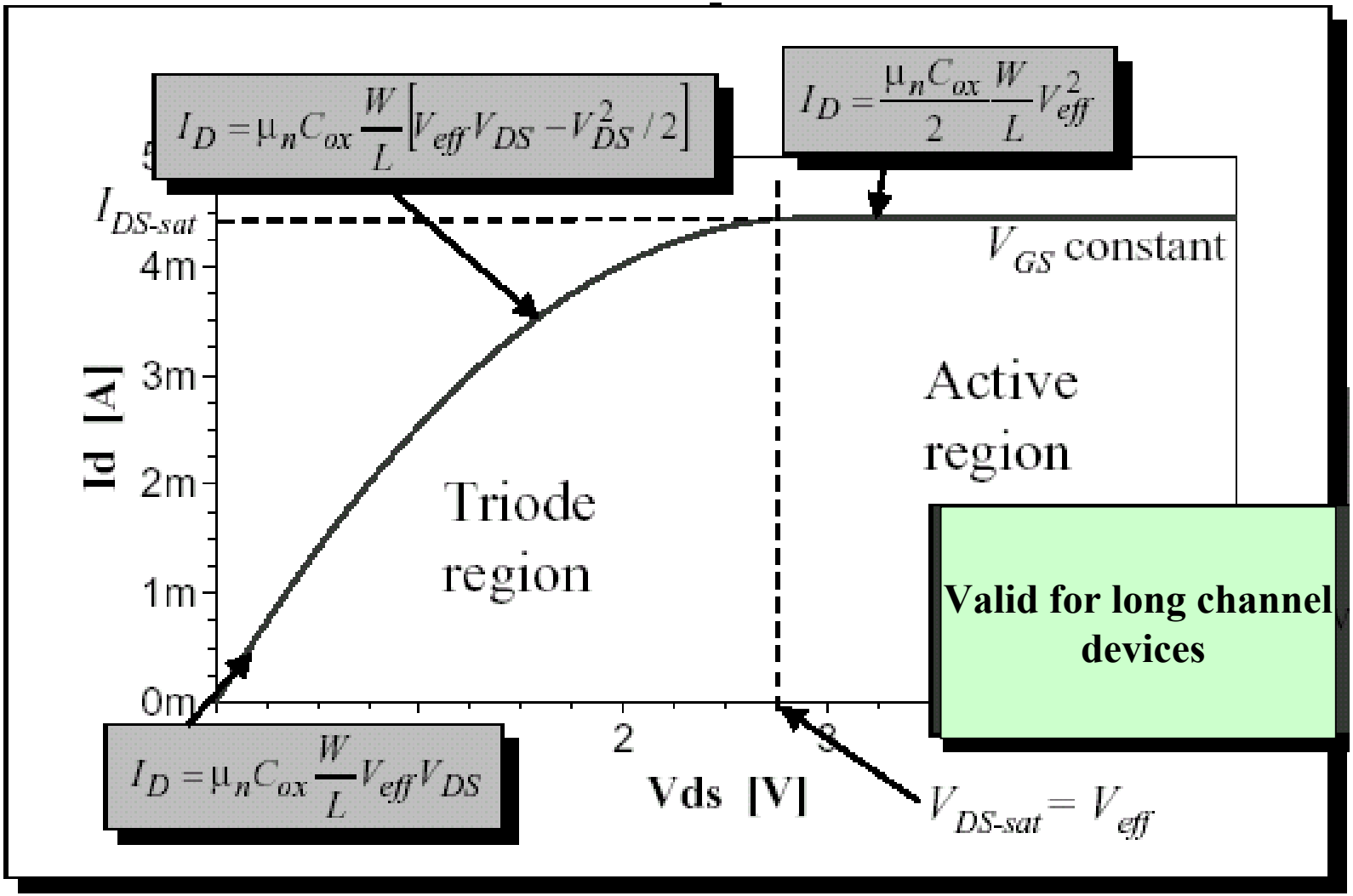
- Integrator



$$v_o(t) = -\frac{g_m}{C}\int^{t} v_{in}(t)dt$$

$$\frac{V_o(s)}{V_{in}(s)} = -\frac{g_m}{Cs}$$

MOS Drain Current Characteristics



CMOS Transconductors

- A large variety of methods
- Best approach depends on application
- Two main classifications
  - Triode or
  - Active based
- Triode-based tends to have better linearity
- Active-based tend to have faster speed for the same operating current

Triode Transconductors

- Recall n-channel triode equation

$$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{GS}-V_{tn})V_{DS}-\frac{V_{DS}^2}{2}\right), \quad (V_{GS} > V_{DS}+V_{tn})$$

- Above models are only reasonably accurate
- Not nearly as accurate as exponential model in BJTs
- Use fully-differential architectures to reduce even order distortion terms. It also improves common mode noise rejection

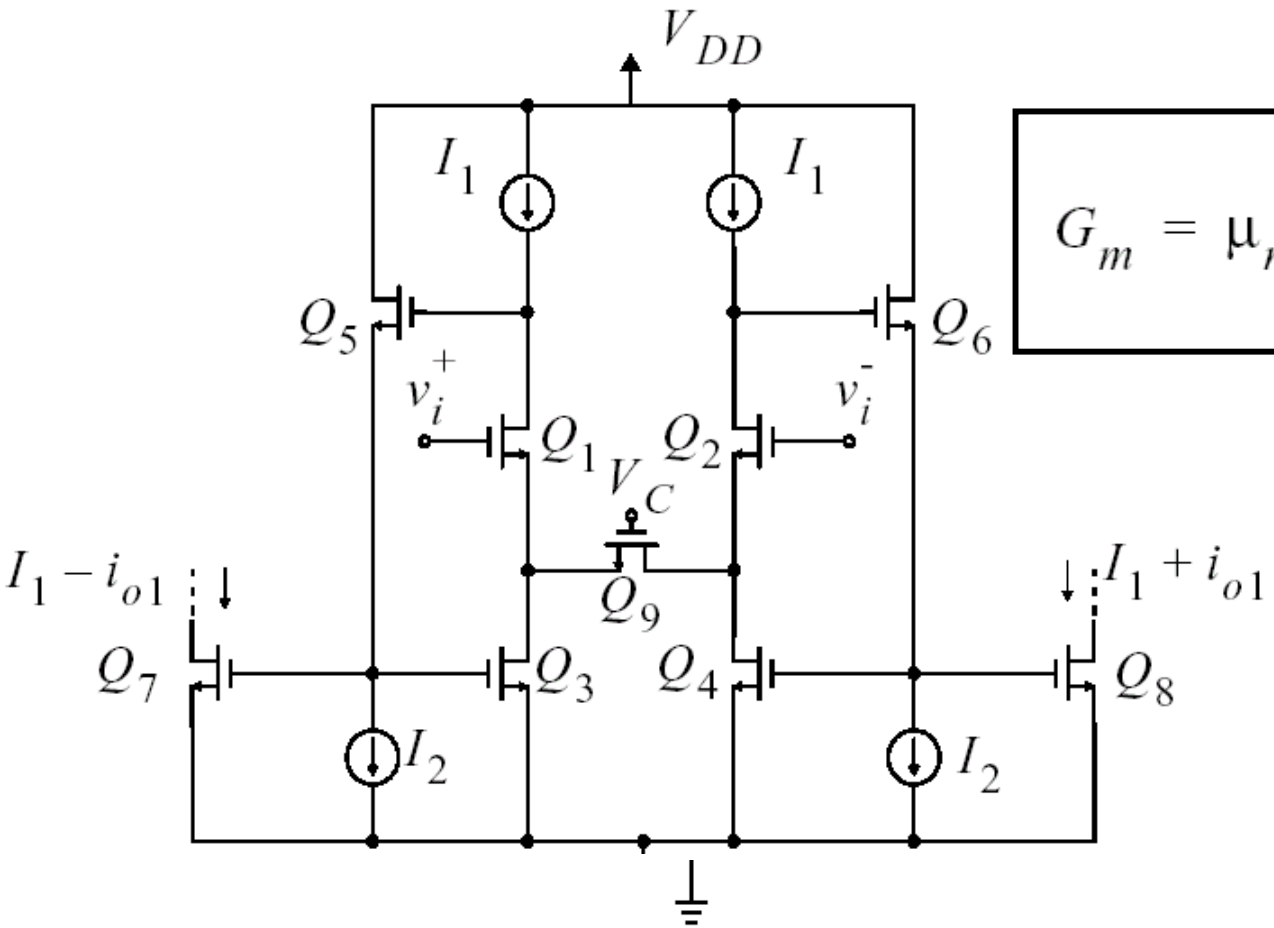
Fixed-Bias Triode Transconductor

- Use a small V_{ds} so the V_{ds}^2 term goes to zero

$$r_{DS} \equiv \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Bigg|_{v_{DS}=0} = \left(\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{tn}) \right)^{-1}$$

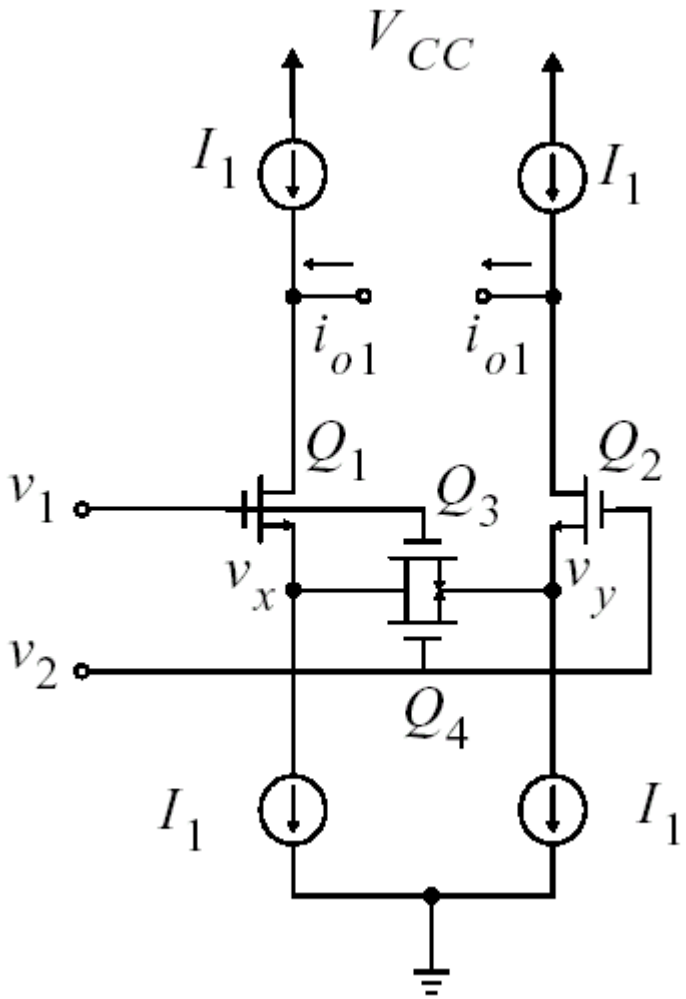
- Can use a triode transistor where a resistor would normally be used.
- Resistance value is tunable

Fixed-Bias Triode Transconductor



$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_9 (v_{gs9} - V_{tn})$$

Varying-Bias Triode Transconductor



$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1+4k_3)\sqrt{k_1}}$$

Varying-Bias Triode Transconductor

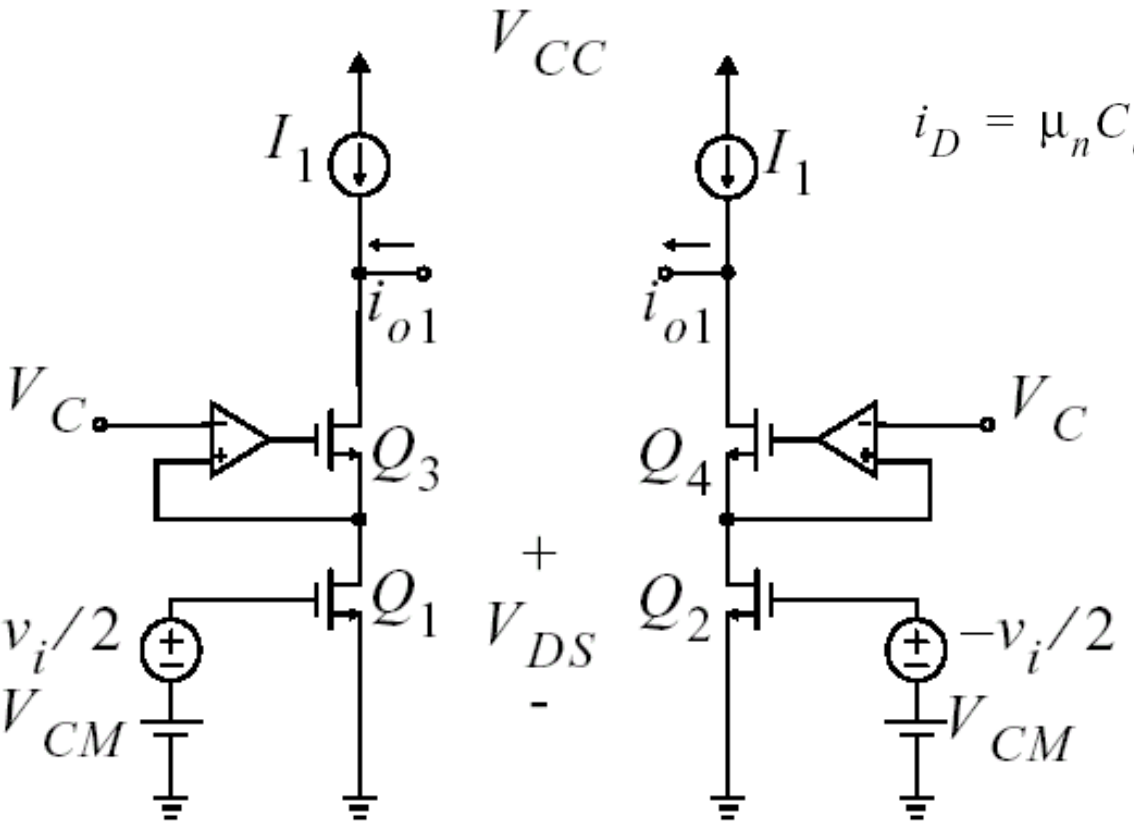
- Gates of $Q3$, $Q4$ connected to the differential input
- $Q3$ and $Q4$ undergo varying bias conditions to improve linearity
- Can show

$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1+4k_3)\sqrt{k_1}}$$

- Note, *Gm* proportional to square-root of I_1

Drain-Source Fixed-Bias Transconductor

- If V_{DS} kept constant wrt V_{GS}, then i_D linear



$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{GS}-V_{tn})V_{DS}-\frac{V_{DS}^2}{2}\right)$$

$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_1 V_{DS}$$

Drain-Source Fixed-Bias Transconductor

- Can realize around 50 dB linearity (not much better since model is not that accurate)
- Requires a fully-differential structure to cancel even order terms
- V_C sets V_{DS} voltage
- Requires a non-zero common-mode voltage on input
- Note that *Gm* roughly proportional to bias current since current roughly proportional to V_{DS}

Active-Based Transconductors

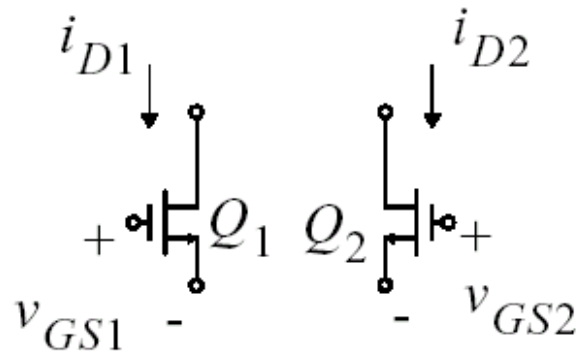
- In active region

$$I_D = K_i(V_{GS} - V_{tn})^2$$

when $V_{DS} \geq V_{GS} - V_{tn} = V_{eff}$ and $V_{GS} \geq V_{tn}$

Here, $K_i \equiv (\mu_n C_{ox}/2)(W/L)_i$

Constant Sum of Gate-Source Voltages



(matched devices)

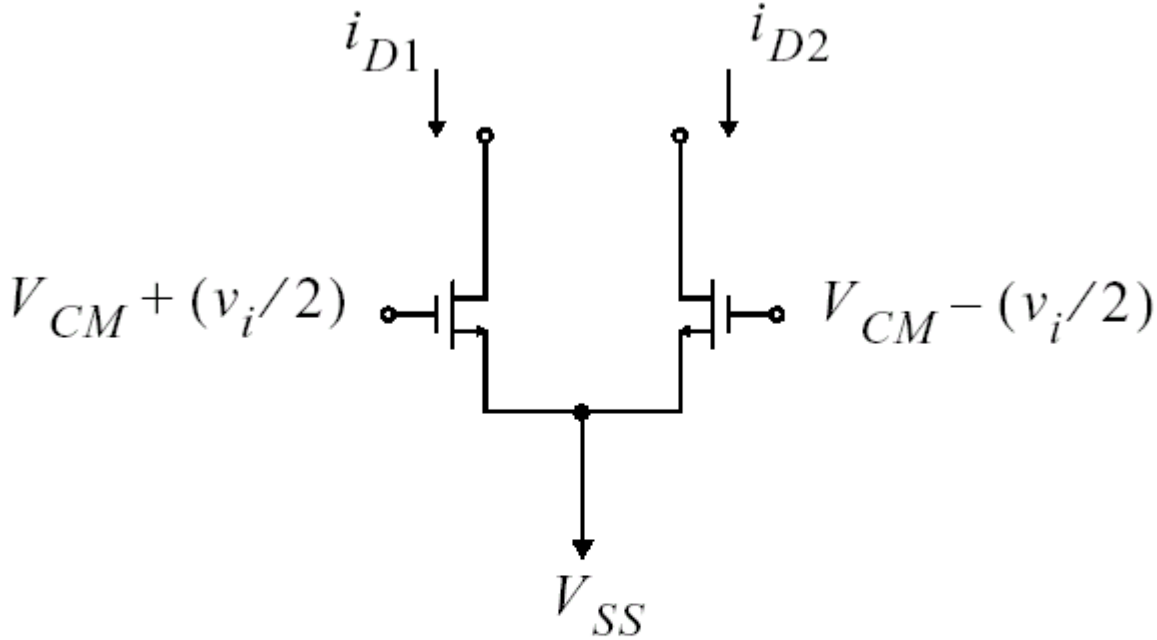
$$(i_{D1} - i_{D2}) = K(v_{GS1} + v_{GS2} - 2V_{tn})(v_{GS1} - v_{GS2})$$

$$K = (\mu_n/2)C_{ox}\left(\frac{W}{L}\right)$$

- If $V_{GS1}+V_{GS2}$ = constant then linear transconductor

Note : Differential output current linear but single ended currents have large second-order distortion.

Source-Connected Differential Pair



$$(i_{D1} - i_{D2}) = 2K(V_{CM} - V_{SS} - V_{tn})(v_i)$$

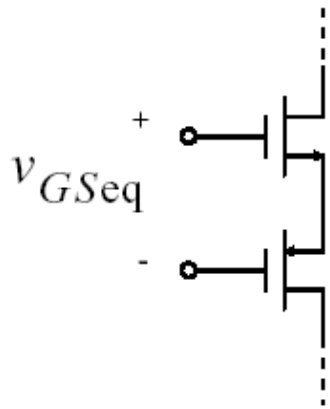
$$G_m = 2K(V_{CM} - V_{SS} - V_{tn})$$

Source-Connected Differential Pair

- Input signal varies symmetrically around a common mode voltage
- Linearity limited due to square-law model being inaccurate
- In addition, even-order harmonics occur if the difference between two drain currents not exact.
- Limited to less than 50 dB linearity
- Adjust G_m by varying V_{CM}
- In a short channel process, velocity saturation limits transconductance variation

Inverter-Based Transconductors

- CMOS Pair



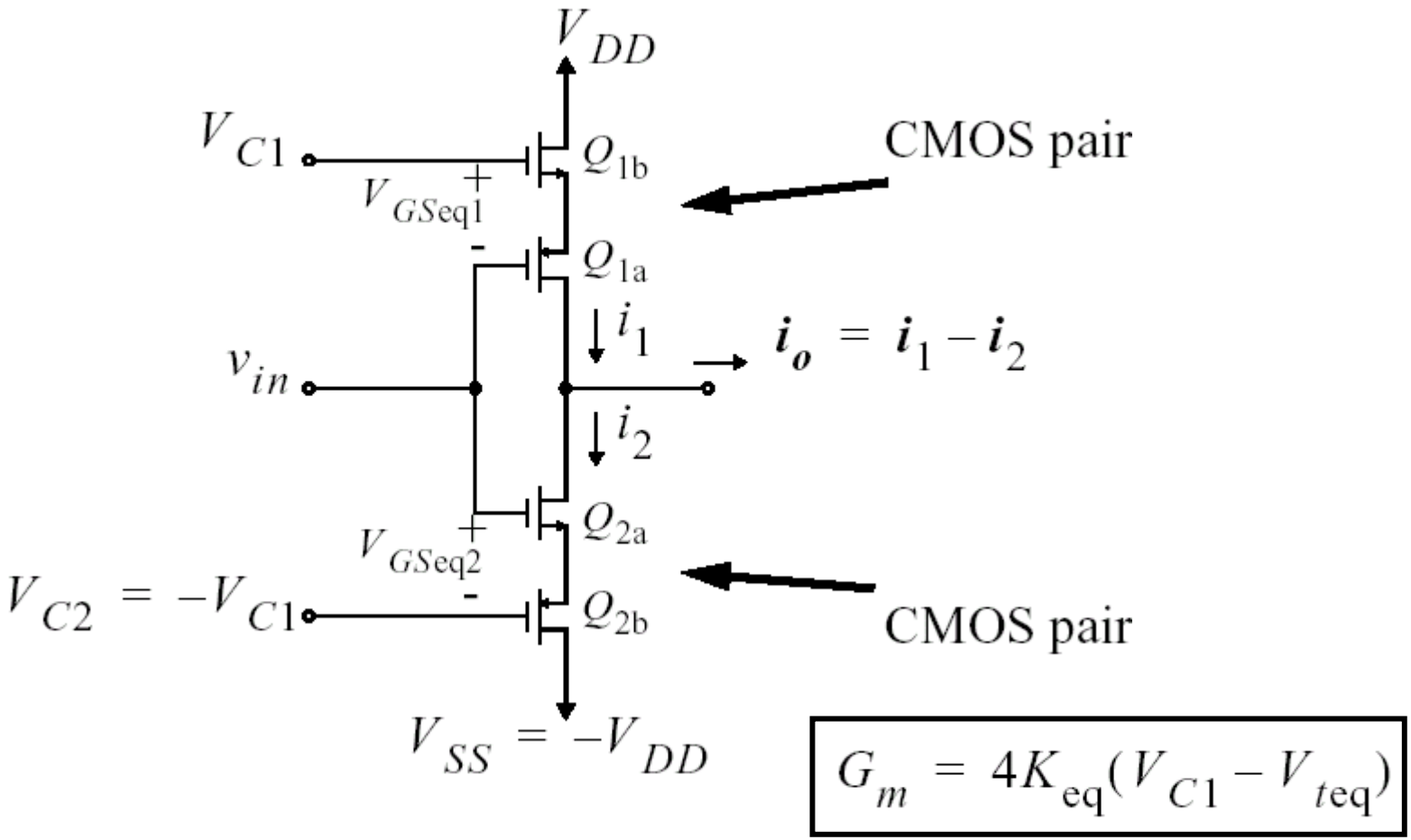
$$i_D = K_{eq}(v_{GSeq} - V_{teq})^2$$

$$K_{eq} = \frac{K_n K_p}{(\sqrt{K_n} + \sqrt{K_p})^2} \qquad V_{teq} = V_{tn} - V_{tp}$$

(where $V_{tn} > 0$ and $V_{tp} < 0$)

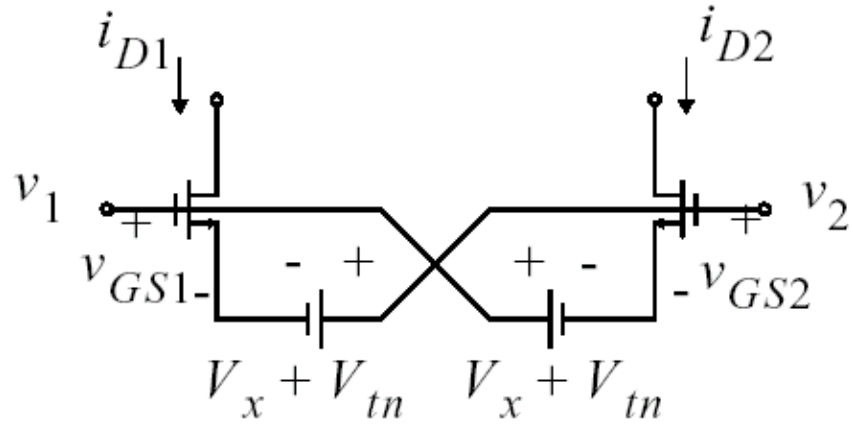
- Above circuit acts as a single transistor with threshold V_{teq} and parameter K_{eq}

Inverter-Based Linear Transconductor



$$G_m = 4K_{eq}(V_{C1} - V_{teq})$$

Diff-Pair with Floating Voltage Sources



$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2)$$

$$G_m = 4KV_x$$

- Writing a voltage equation around the loop

$$v_{GS1} - (V_x + V_{tn}) + v_{GS2} - (V_x + V_{tn}) = 0$$

- Implying:

$$v_{GS1} + v_{GS2} = 2(V_x + V_{tn})$$

- Thus, a constant sum of gate-source voltages occurs even if input signal is not balanced

Diff-Pair with Floating Voltage Sources

$$v_1 - v_{GS1} + V_x + V_{tn} = v_2$$
$$v_2 - v_{GS2} + V_x + V_{tn} = v_1$$

- By Subtracting we obtain

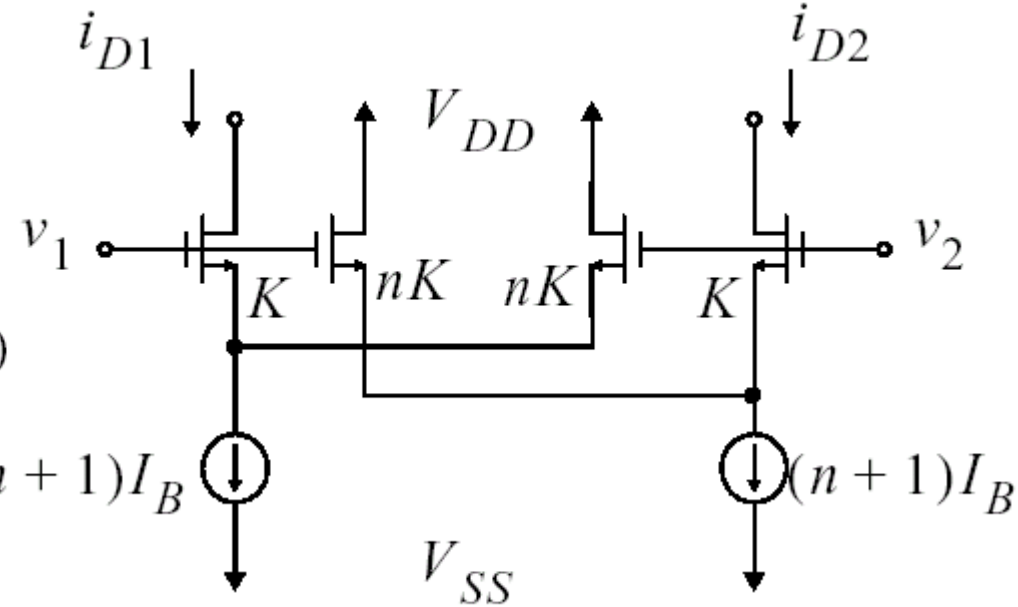
$$v_{GS1} - v_{GS2} = 2(v_1 - v_2)$$

- Finally, output differential current:

$$(i_{D1} - i_{D2}) = 4KV_x(v_1 - v_2)$$

Diff-Pair with Floating Voltage Sources

- Approach #1:



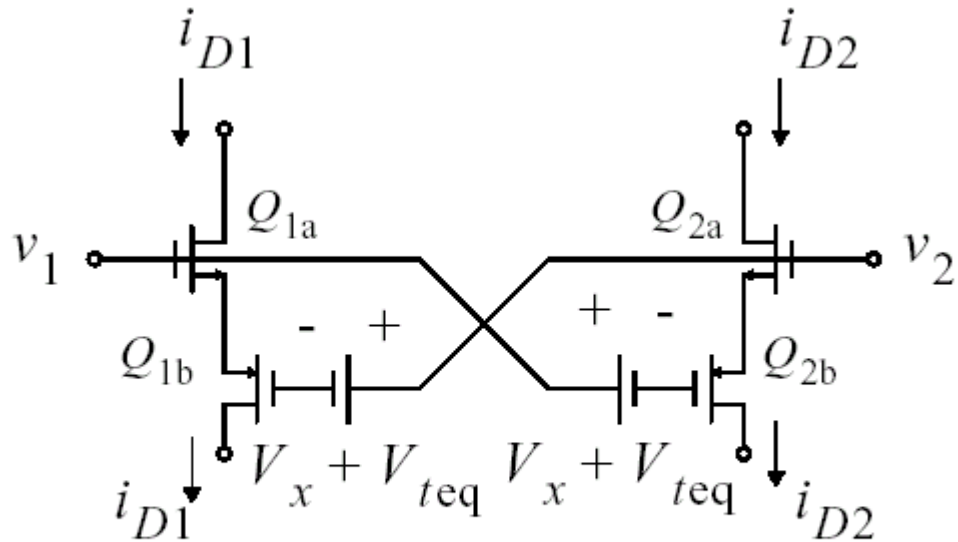
$$(i_{D1} - i_{D2}) = \left(\frac{n}{n+1}\right) 4\sqrt{KI_B}(v_1 - v_2)$$

$$G_m = \left(\frac{n}{n+1}\right) 4\sqrt{KI_B}$$

- Floating voltage sources built using large transistors (n> 5)
- Disadvantage — large bias current and moderate linearity

Diff-Pair with Floating Voltage Sources

- Approach #2

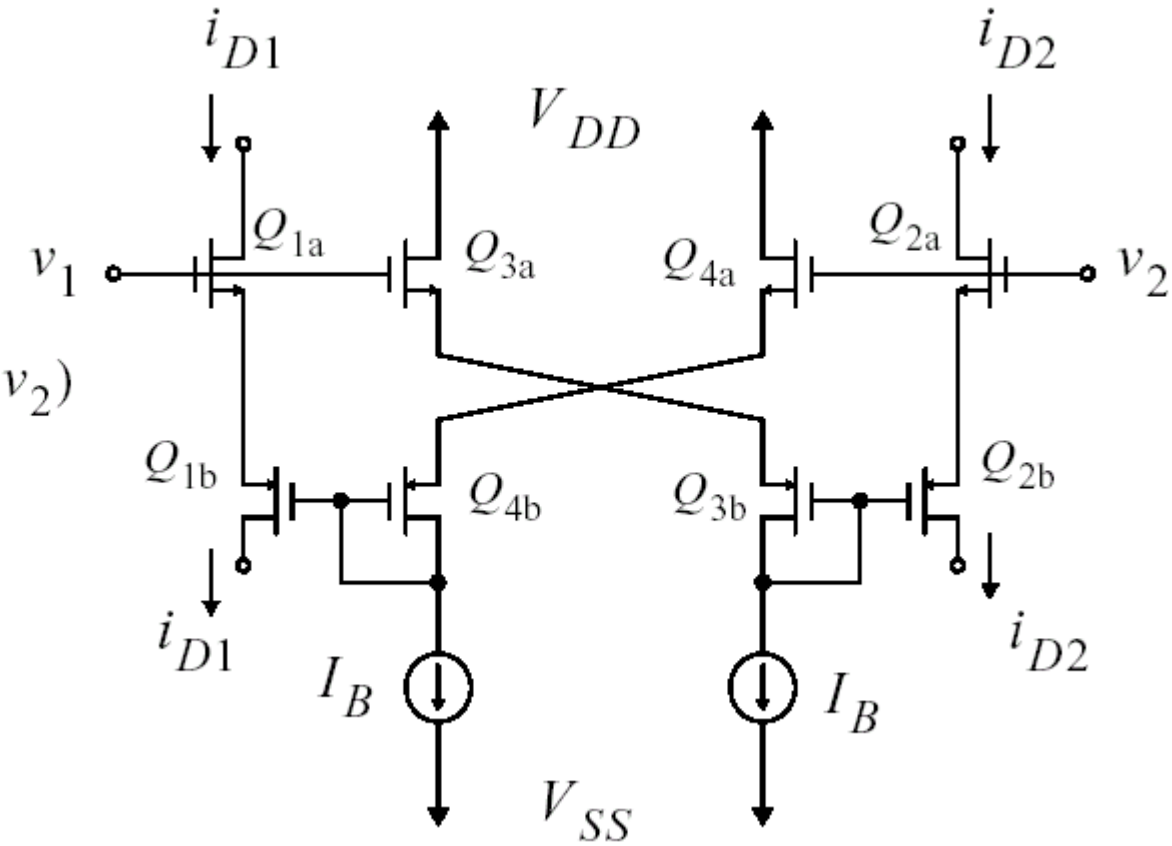


$$(i_{D1} - i_{D2}) = 4K_{eq}V_x(v_1 - v_2)$$

- Replace diff-pair transistors with CMOS pairs
- Now replace floating voltage sources with CMOS

Diff-Pair with Floating Voltage Sources

- Approach #2:

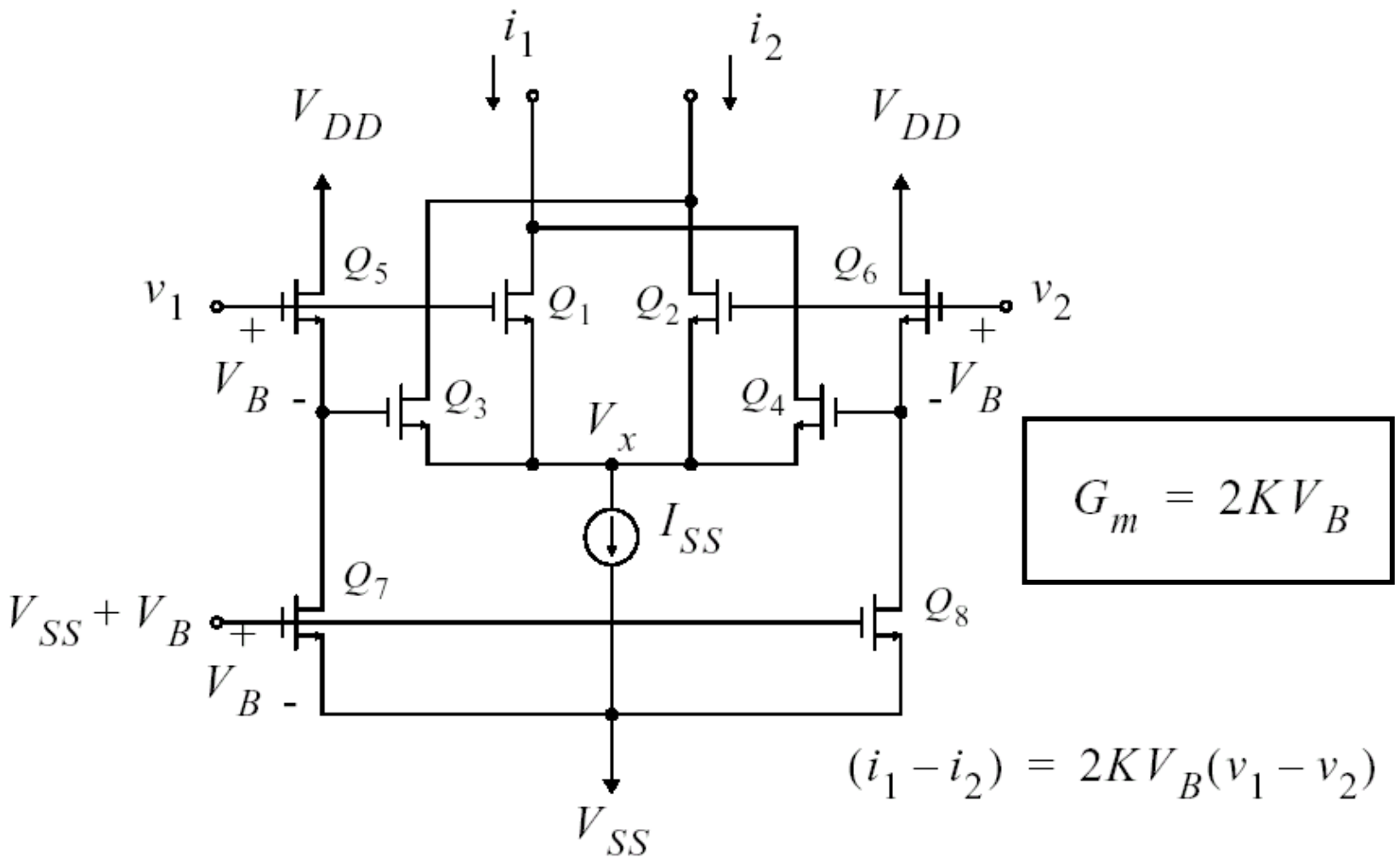


$$(i_{D1} - i_{D2}) = 4\sqrt{K_{eq} I_B}(v_1 - v_2)$$

$$\boxed{G_m = 4\sqrt{K_{eq} I_B}}$$

- G_m proportional to $\sqrt{I_B}$
- Requires a large power supply

Bias-Offset Cross-Coupled Diff-Pairs



$$G_m = 2KV_B$$

$$(i_1 - i_2) = 2KV_B(v_1 - v_2)$$

Bias-Offset Cross-Coupled Diff-Pairs

$$i_1 = K(v_1 - V_x - V_{tn})^2 + K(v_2 - V_B - V_x - V_{tn})^2$$

$$i_2 = K(v_2 - V_x - V_{tn})^2 + K(v_1 - V_B - V_x - V_{tn})^2$$

$$(i_1 - i_2) = 2KV_B(v_1 - v_2)$$

- The output differential current is linear with respect to differential input voltage
- G_m proportion to V_B which is proportional to $\sqrt{I_B}$
- Bias current, I_{SS}, does not affect *Gm* but does set maximum (or minimum) output current available