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EEE598D: Analog Filters & Signal Processing Circuits

Instructor:

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Today: Introduction to Gm-C Circuits (II)

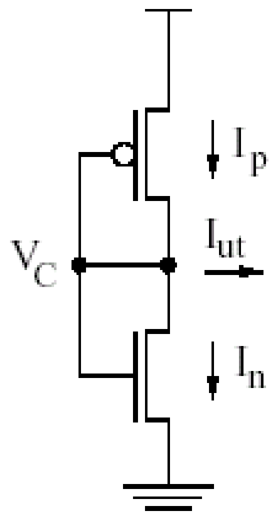
- MOS linear transconductor realization techniques (Con’t)
- Tuning of Gm-C filters

CMOS Inverter-Based Transconductor

- An inherently symmetric transconductor
  - Symmetry is used to cancel inverter nonlinearities
- Theoretically infinite bandwidth
  - No internal nodes => no parasitic poles => bandwidth limited only by non-quasi-static behavior of transistor
- Theoretically infinite (differential) DC gain
  - Negative resistance, for differential signals, in parallel with output resistance makes Rout very high => high gain

Common-Mode Voltage For Inverter

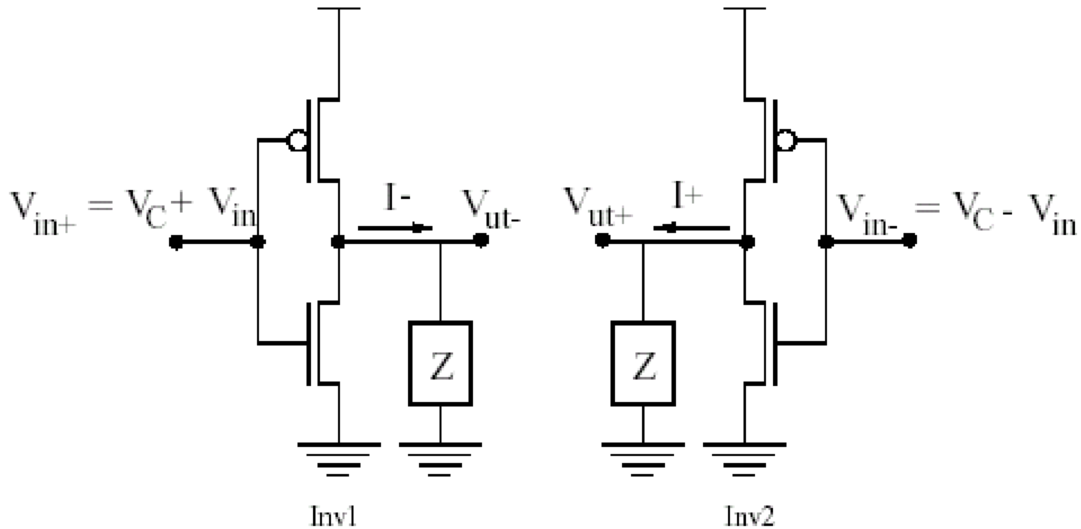
- Used to guarantees the output current to be zero even when input and output are not connected.



$$0 = I_{ut} = I_p - I_n = \frac{1}{2}\beta_p(V_{DD} - V_C - |V_{T_p}|)^2 - \frac{1}{2}\beta_n(V_C - V_{T_n})^2$$

$$V_C = \frac{V_{DD} - |V_{T_p}| + \alpha V_{T_n}}{1 + \alpha} \qquad \alpha = \sqrt{\frac{\beta_n}{\beta_p}}$$

Balanced inverter pair



If voltage on input is $V_C + V_{in}$

$$I_{outp} = \frac{1}{2}\beta_p(V_{DD} - V_C - |V_{T_p}| - V_{in})^2 - \frac{1}{2}\beta_n(V_C - V_{T_n} + V_{in})^2$$

If voltage on input is $V_C - V_{in}$

$$I_{outm} = \frac{1}{2}\beta_p(V_{DD} - V_C - |V_{T_p}| + V_{in})^2 - \frac{1}{2}\beta_n(V_C - V_{T_n} - V_{in})^2$$

Balanced Inverter Pair (cont')

That is we have:

$$I_{outp} = \frac{\beta_p}{2}(a - V_{in})^2 - \frac{\beta_n}{2}(b + V_{in})^2 = -V_{in}(\beta_p a + \beta_n b) + V_{in}^2\left(\frac{\beta_p - \beta_n}{2}\right) + \frac{\beta_p}{2}a^2 - \frac{\beta_n}{2}b^2$$

$$I_{outm} = \frac{\beta_p}{2}(a + V_{in})^2 - \frac{\beta_n}{2}(b - V_{in})^2 = V_{in}(\beta_p a + \beta_n b) + V_{in}^2\left(\frac{\beta_p - \beta_n}{2}\right) + \frac{\beta_p}{2}a^2 - \frac{\beta_n}{2}b^2$$

with $a = V_{DD} - V_C - \left|V_{T_p}\right|$ *and* $b = V_C - V_{T_n}$

The differential output current (defined into the circuit) is:

$$I_{out} = I_{outm} - I_{outp} = 2V_{in}(\beta_p a + \beta_n b) = (V_{inp} - V_{inm})(\beta_p a + \beta_n b) = g_{md} V_{ind}$$

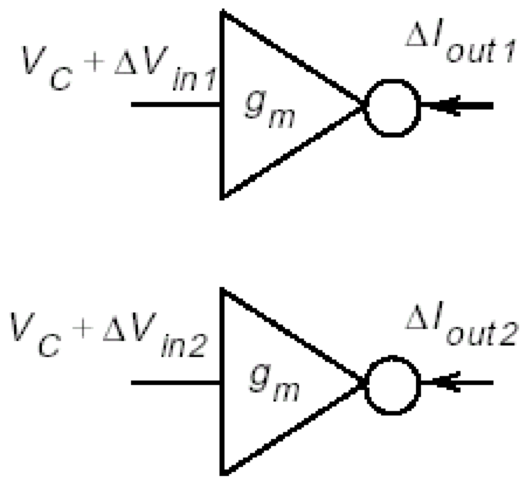
$$g_{md} = \beta_p(V_{DD} - V_C - \left|V_{T_p}\right|) + \beta_n(V_C - V_{T_n}) = (V_{DD} - \left|V_{T_p}\right| - V_{T_n})\sqrt{\beta_n \beta_p}$$

Transconductance can be tuned at run time by changing V_{DD}

Output Resistance

- Basic symmetric V-I converter

Basic symmetric V-I converter



Voltage variations around V_C result in linear change in current around $I_{outQ}=0$

$$g_m \Delta V_{inx} = \Delta I_{outx}$$

Internal output resistance of inverter turns this current variation in to a voltage variation (around V_C):

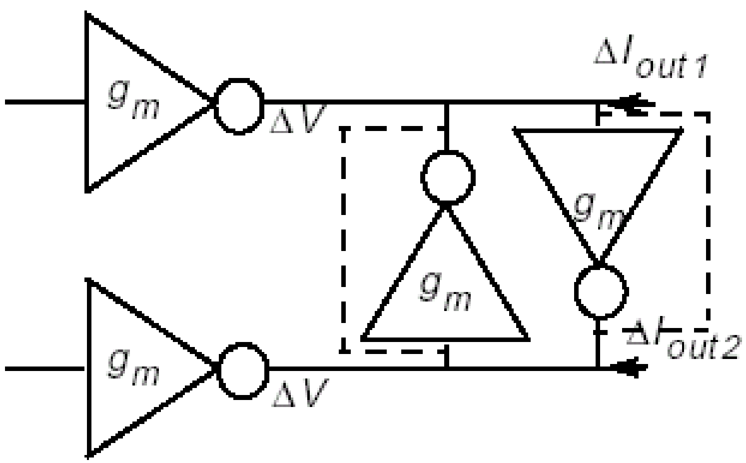
$$\Delta V_{outx} = r_{outInv} \Delta I_{outx}$$

r_{outInv} is transistor output resistances in parallel: $1/(g_{dp}+g_{dn})$

Remember: output conductance is much smaller than transconductance

Output Resistance (Cont')

Common-mode case

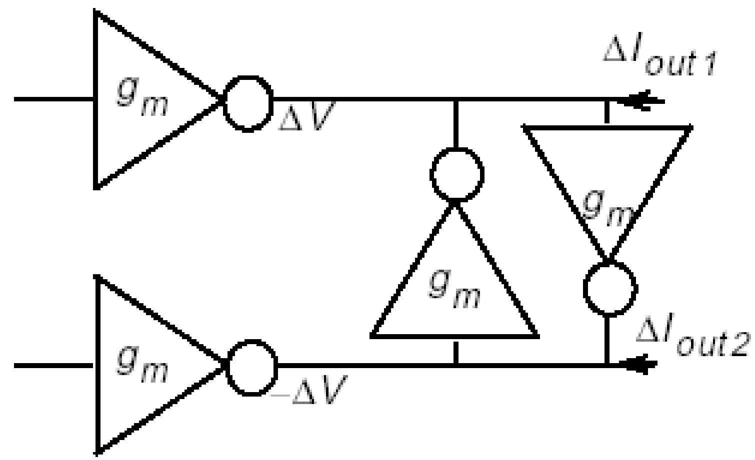


Voltage changes on input and output of load inverters go the same way: it is as if the inverters where shorted:

$$\Delta I_{out1} = g_m \Delta V$$

$$r_{outCM1} = \frac{1}{g_m}$$

Differential-mode case



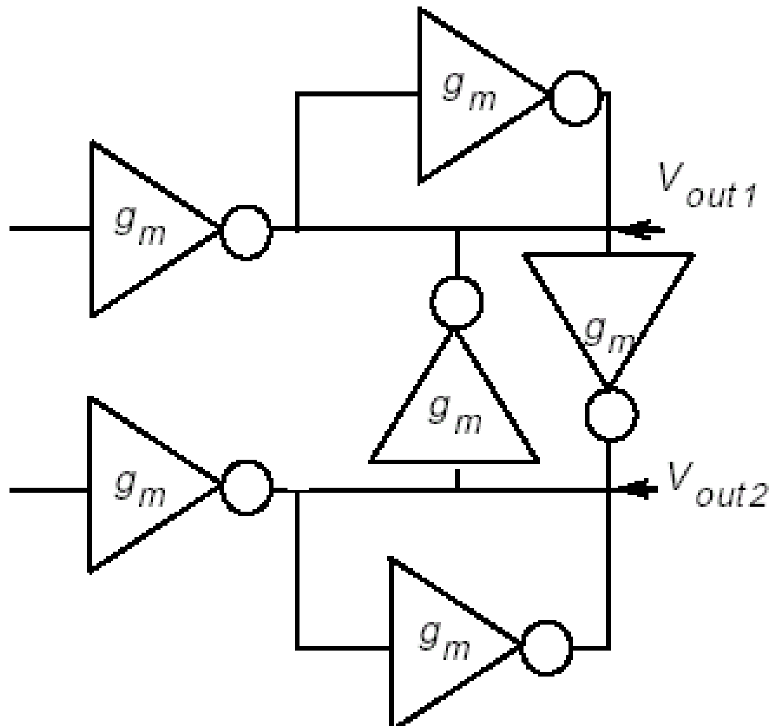
Voltage changes go opposite ways current change has opposite sign from CM case

$$\Delta I_{out1} = -g_m \Delta V$$

$$r_{outDM1} = -\frac{1}{g_m}$$

Note output conductances are ignored here as they are much smaller than g_m

Output Resistance (Cont')

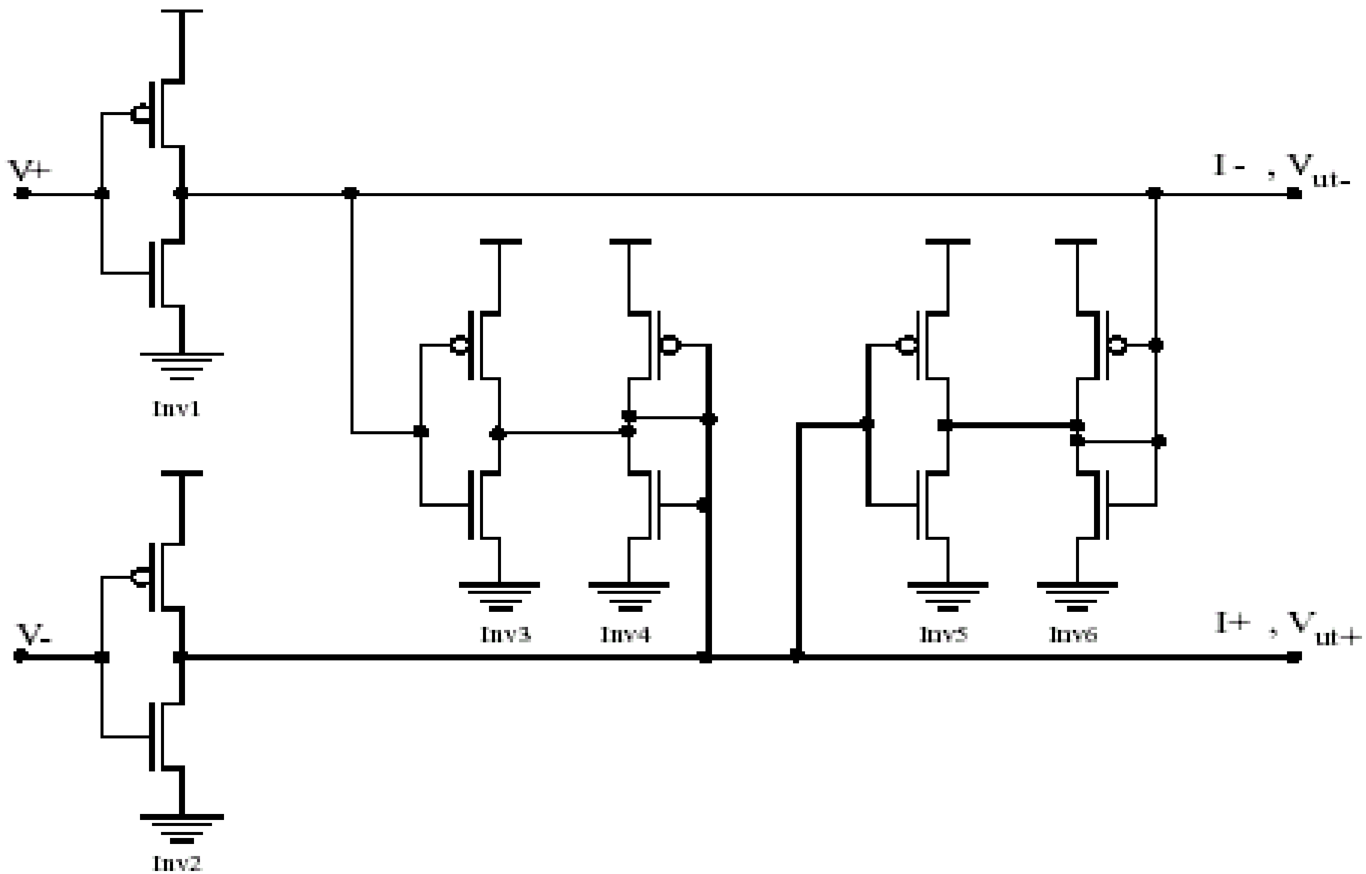


Ideally: $r_{outDM1} = r_{outDM,2} = \dfrac{1}{3g_{oi} + g_m - g_m} = \dfrac{1}{3g_{oi}}$

$$r_{outCM1} = r_{outCM,2} = \frac{1}{3g_{oi} + g_m + g_m} = \frac{1}{3g_{oi} + 2g_m}$$

In reality transistor sizes (at design time), or V_{DD}s (at run time) have to be tuned.

Differential Transconductance Stage



Transfer Function

- Assume a similar transconductor as load. Small-signal transfer function can be derived as:

$$H(s) = \frac{\dfrac{1}{3(g_{d_n} + g_{d_p})}}{1 + s\dfrac{3(C_{gs_n} + C_{gs_p})}{3(g_{d_n} + g_{d_p})}} = \frac{1}{3}\frac{g_{m_n} + g_{m_p}}{g_{d_n} + g_{d_p} + s(C_{gs_n} + C_{gs_p})}$$

With non-quasi-static phenomena, distributed expressions

$$g_d \Rightarrow \frac{g_d}{1 + s\tau_1} \qquad g_m \Rightarrow \frac{g_m}{1 + s\tau_1} \qquad C_{gs} \Rightarrow C_{gs}\frac{1 + s\tau_2}{1 + s\tau_1}$$

$$\text{with} \quad \tau_1 = \frac{4}{15}\tau_o \quad \tau_2 = \frac{2}{15}\tau_o \quad \text{and} \quad \tau_o = \frac{3}{2}\tau_T = \frac{3}{2}\frac{C_{gs}}{g_m}$$

$$H(s) = \frac{N(s)}{D(s)} = \frac{1}{3}\frac{\dfrac{g_{m_n}}{1 + s\tau_{1n}} + \dfrac{g_{m_p}}{1 + s\tau_{1p}}}{\dfrac{g_{d_n}}{1 + s\tau_{1n}} + \dfrac{g_{d_p}}{1 + s\tau_{1p}} + s\left(C_{gs_n}\dfrac{1 + s\tau_{2n}}{1 + s\tau_{1p}} + C_{gs_p}\dfrac{1 + s\tau_{2p}}{1 + s\tau_{1p}}\right)}$$

Stability Problem

Now, we assume that $L_n=L_p$ and $W_p=\alpha W_n$ with α chosen such that $g_{mn}=g_{mp}$

We then also have: $C_{gsp}=\alpha C_{gsn}$ which makes $\tau_{1p}=\alpha\tau_{1n}$, $\tau_{2p}=\alpha\tau_{2n}$

We also use: $g_{dp}=\alpha g_{dn}$ which makes the calculations somewhat easier

Resulting transfer function:

$$\frac{2g_m}{3g_d(1+\alpha)}\,\frac{1+s\tau_1\frac{(1+\alpha)}{2}}{1+s\tau_1\frac{2\alpha}{1+\alpha}+sA_0\frac{3C_{gs}}{2g_m}[(1+\alpha)+s(2\alpha\tau_1+(1+\alpha^2)\tau_2)+s^2(\alpha+\alpha^2)\tau_1\tau_2]}$$

$\frac{2g_m}{3g_d(1+\alpha)}=A_0$, $\frac{3C_{gs}}{2g_m}=\tau_0$

$$\tau_1 = \frac{4}{15}\tau_o \qquad \tau_2 = \frac{2}{15}\tau_o$$

$$H(s) = \frac{1+s\frac{8}{15}\tau_o}{1+s\left(\frac{2}{5}+4A_o\right)+s^2\frac{44}{15}A_o\tau_o^2+s^3\frac{96}{225}A_o\tau_o^3}$$

Stability Problem

If A_0 is large enough H(s) has a dominant pole at

$$\omega_{p1} \approx \frac{1}{4A_0}\frac{1}{\tau_0}$$

The nondominant poles are at:

$$\omega_{p2} \approx \frac{15}{11}\frac{1}{\tau_0} \approx \frac{1.36}{\tau_0} \qquad \omega_{p3} \approx \frac{44 \cdot 15}{96}\frac{1}{\tau_0} \approx \frac{6.87}{\tau_0}$$

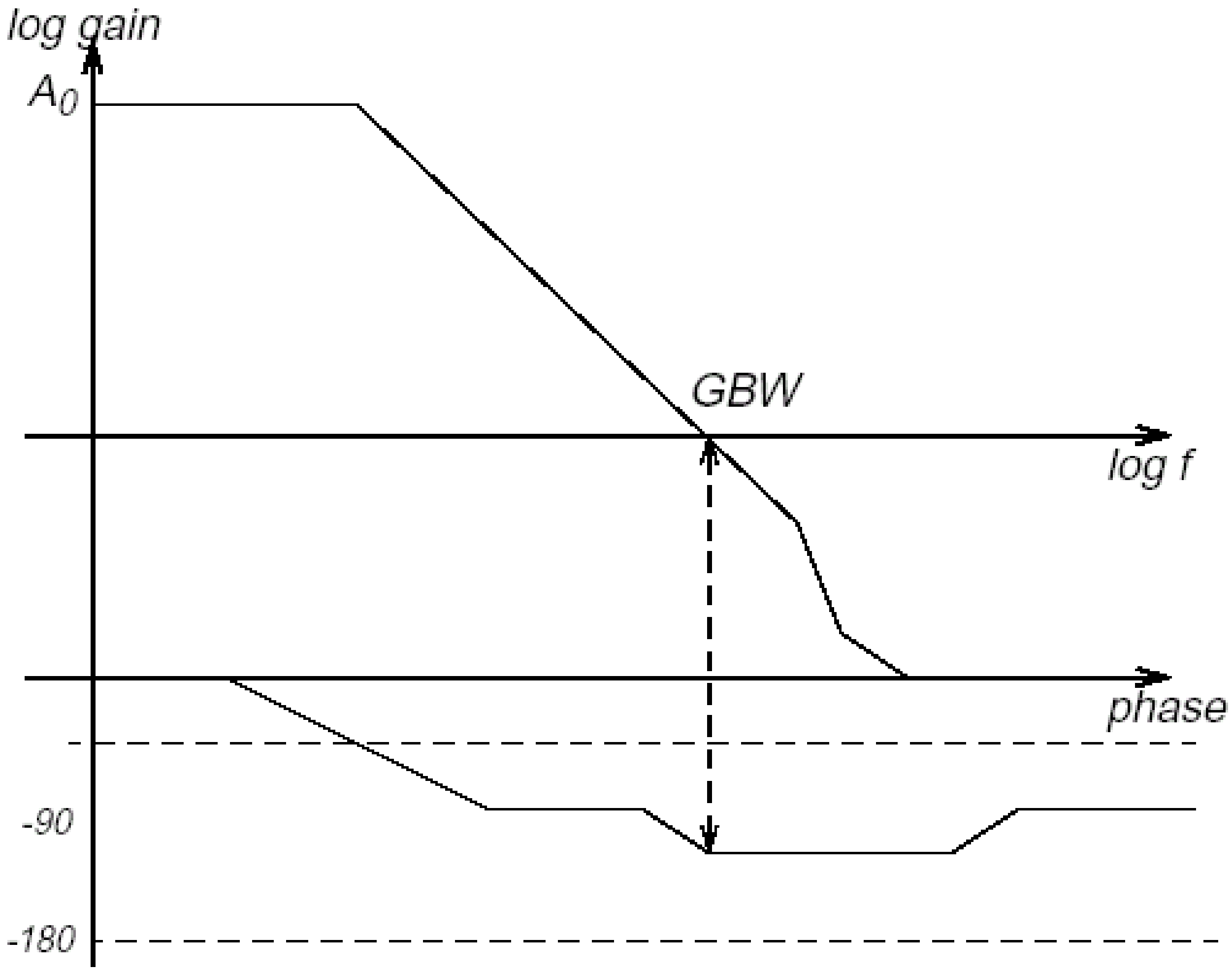
The zero is at: gain-bandwidth product:

$$\omega_Z = \frac{15}{8}\frac{1}{\tau_0} \approx \frac{1.87}{\tau_0} \qquad GBW = \frac{A_0}{4A_0}\frac{1}{\tau_0} = \frac{0.25}{\tau_0}$$

Because $\omega_{p2} < \omega_Z$ the result is a negative phase "blip"

Because $\omega_{p2}/10$ is less than GBW the
phase margin at GBW will be affected and will
be less than 90 degrees => not good for stability
Solution: use a lower A0 to move ω_{p1} closer to ω_{p2}

Bode Plots



Tuning of Gm-C Filters

- Tuning can often be the MOST difficult part of a continuous-time integrated filter design
- Tuning required for CT integrated filters to account for capacitance and transconductance variations - 30% time-constant variations
- Must account for process, temperature, aging, etc.
- While absolute tolerances high, ratio of two like components can be matched to under 1%

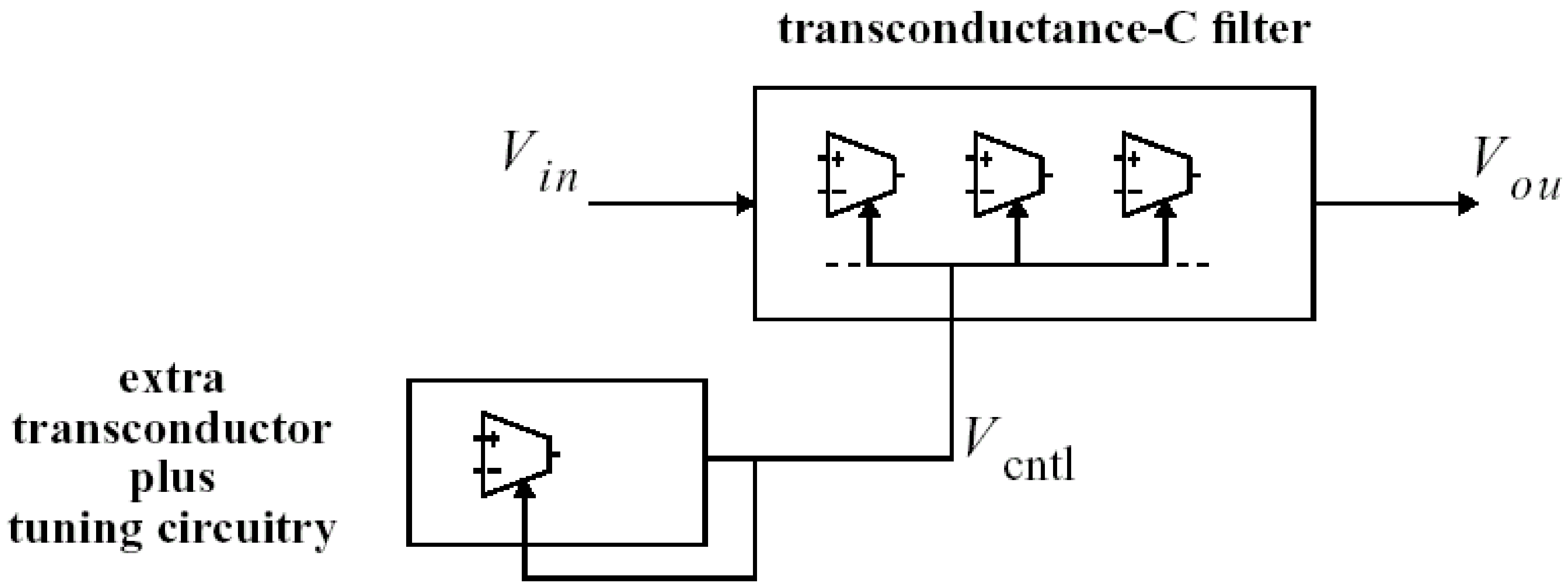
Types of Tuning

- Q tuning
  - DC gain of integrator fine-tuning at run time
- F-tuning
  - For correct frequency response also the cutoff frequency
- Can be combined and controlled by VCO
  - F- tuning by phase-locked loop
  - Q-tuning (which must be faster) by automatic tuning (no loop)

Indirect Tuning

- Most common method — build extra transconductor and tune it
- Same control signal is sent to filter's transconductors which are scaled versions of tuned extra
- Indirect since actual filter's output not measured

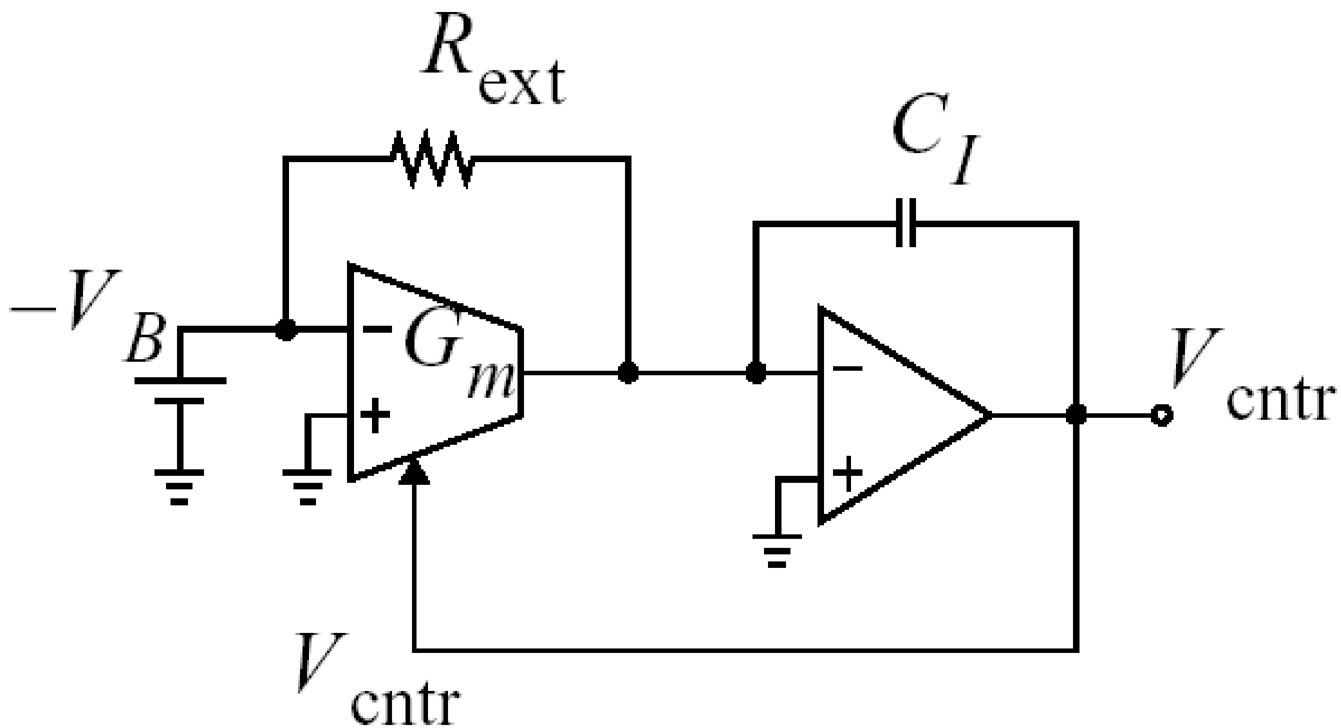
Indirect Tuning



Gm Tuning

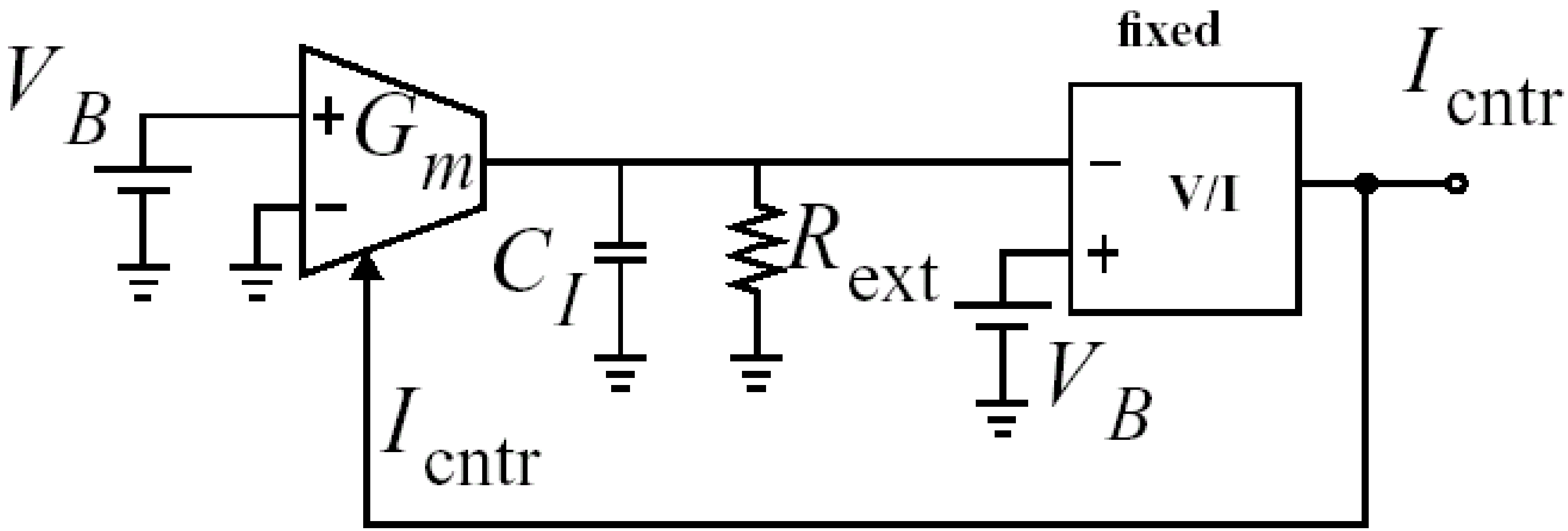
- Can tune Gm to off-chip resistance and rely on capacitor absolute tolerance to be around 10%
- External resistance may be replaced by SC equivalent

Gm Tuning



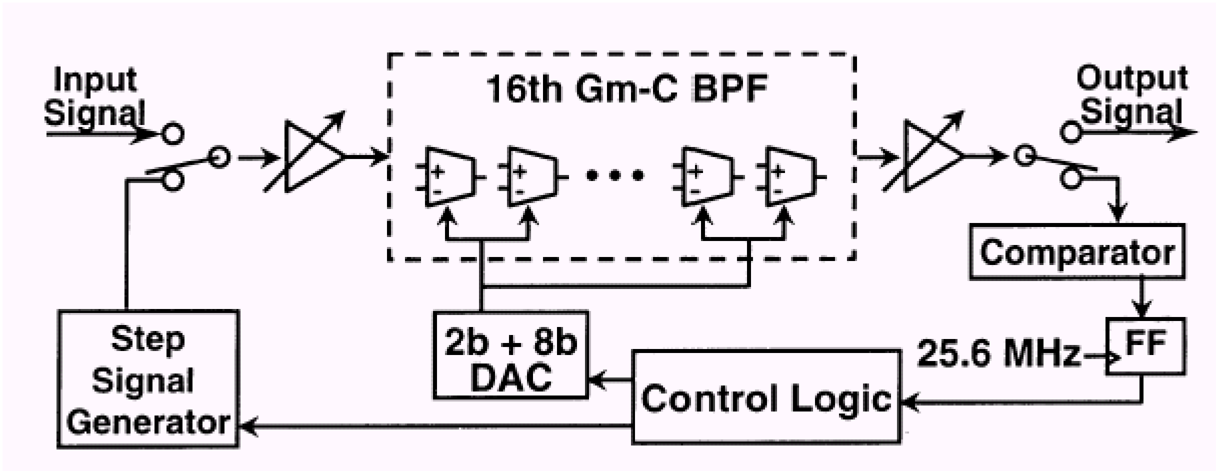
$$G_m = \frac{1}{R_{ext}}$$

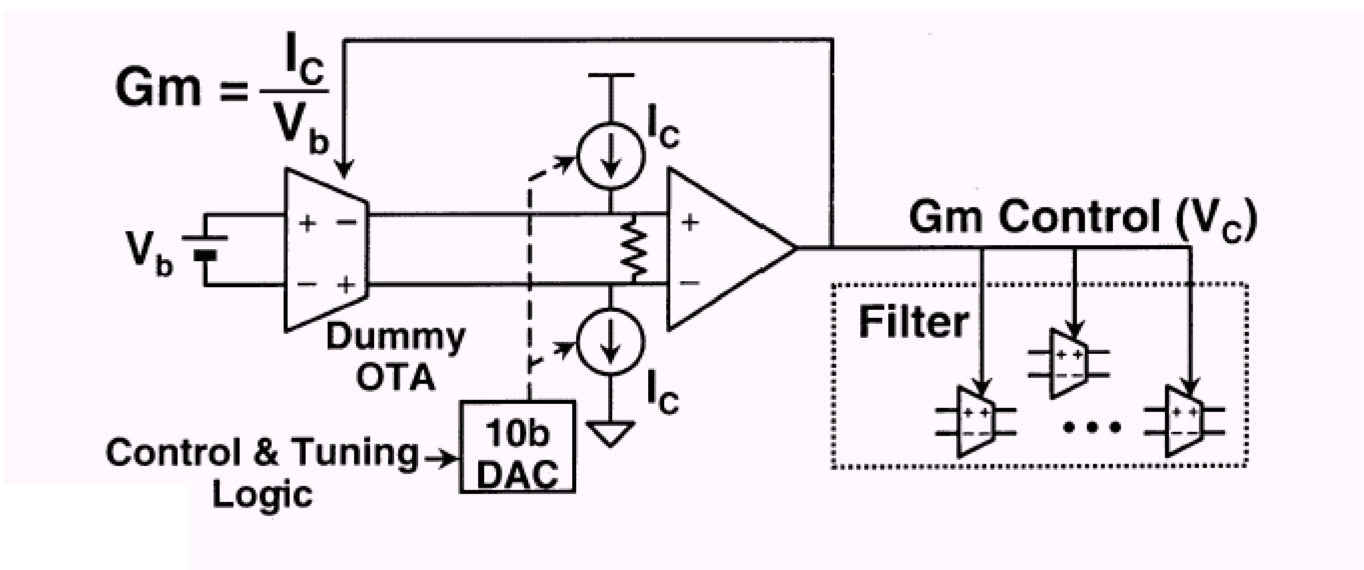
Gm Tuning



$$G_m = \frac{1}{R_{ext}}$$

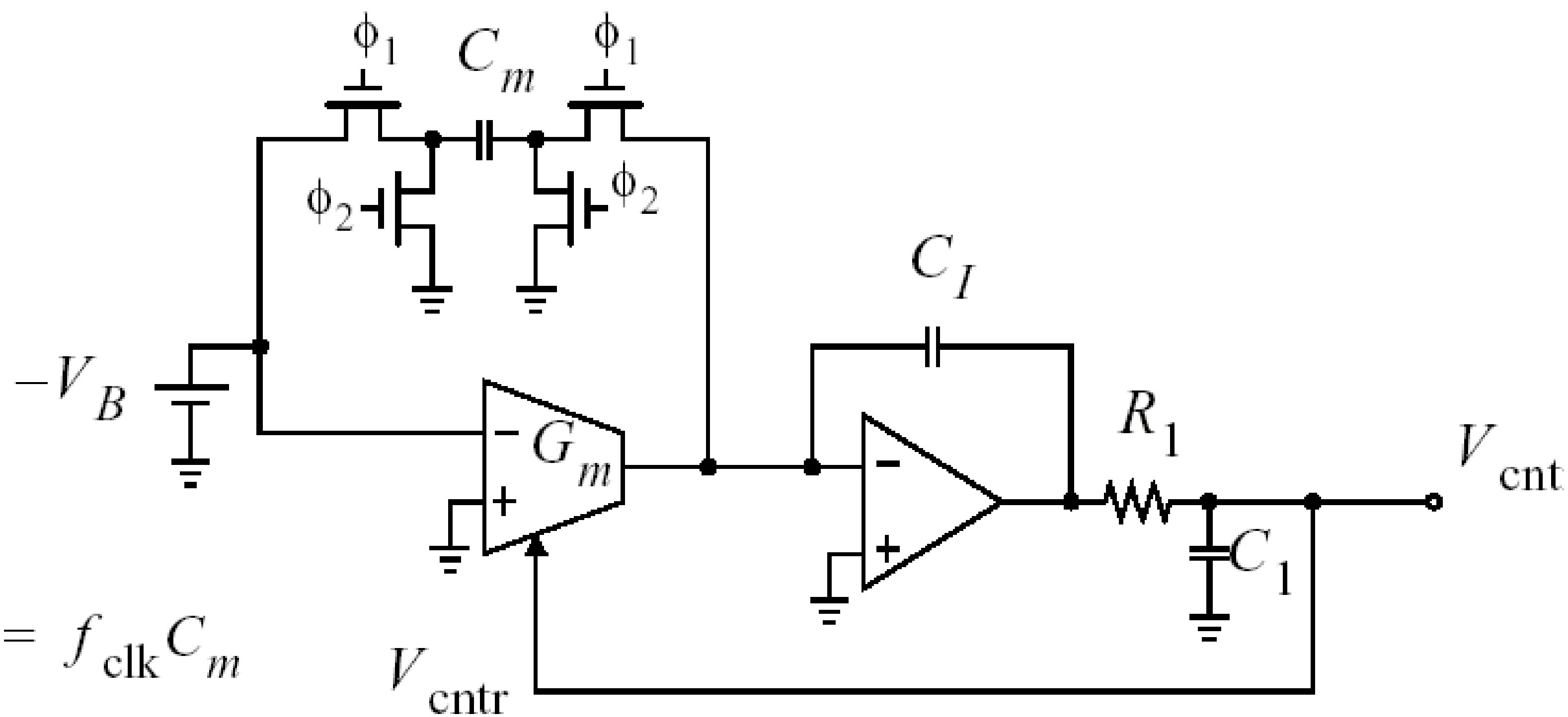
Gm Tuning


Input Signal
16th Gm-C BPF
Output Signal
Comparator
FF
25.6 MHz
Step Signal Generator
2b + 8b DAC
Control Logic


Gm = Ic / Vb
Ic
Vb
Dummy OTA
Gm Control (Vc)
Filter
Control & Tuning Logic
10b DAC

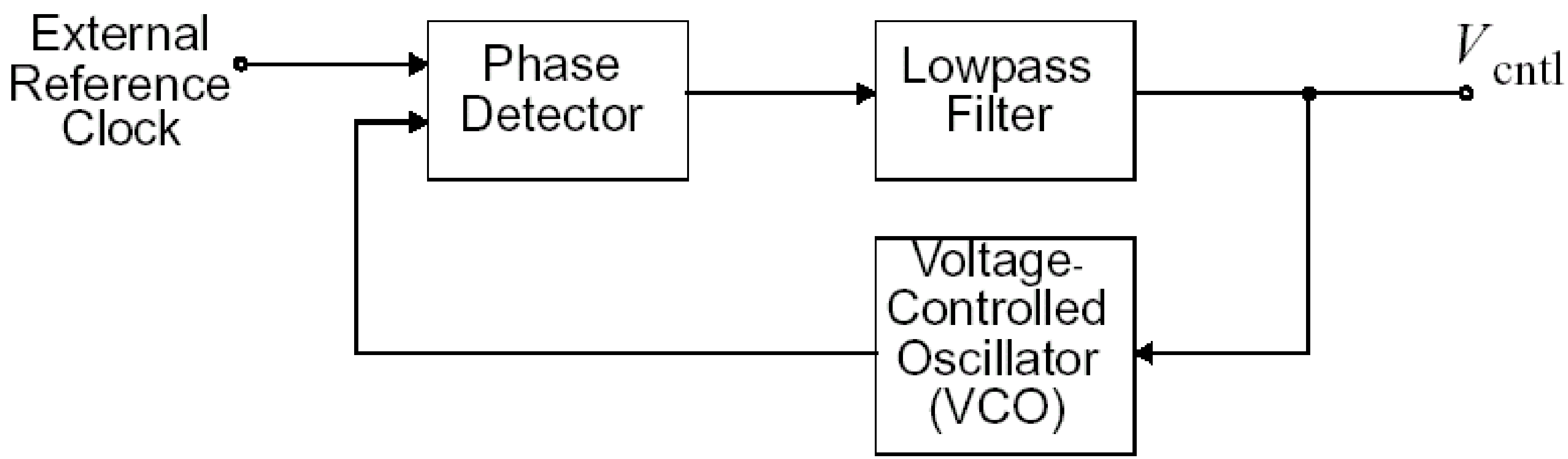
Frequency Tuning

- A precise ratio *Gm/ C* set — time period needed
- External resistance replaced by SC equivalent



$$G_m = f_{clk} C_m$$

Frequency Tuning



Frequency Tuning

- Use a PLL to tune 2 integrators which realize a VCO
- Once VCO set to external frequency, then *Gm/ C* of VCO is set to correct value
- Choice of external clock frequency is difficult.
  - Leaks into filter if within passband
  - Poor matching if too far from passband

Q-Factor Tuning

- Most industrial applications do not presently use Q tuning and rely on matching
- For very high-performance circuits, may have to also tune Q-factor as well as *Gm /C* ratio
- Can use a magnitude locked-loop
- Can use adaptive filtering techniques where filter output is directly observed
- Example: look at step response for a square-wave type input (i.e. digital transmission signal)
  - slope determined by time-constant
  - peak determined by Q-factor

Tuning Circuit Technique: Phase Detect

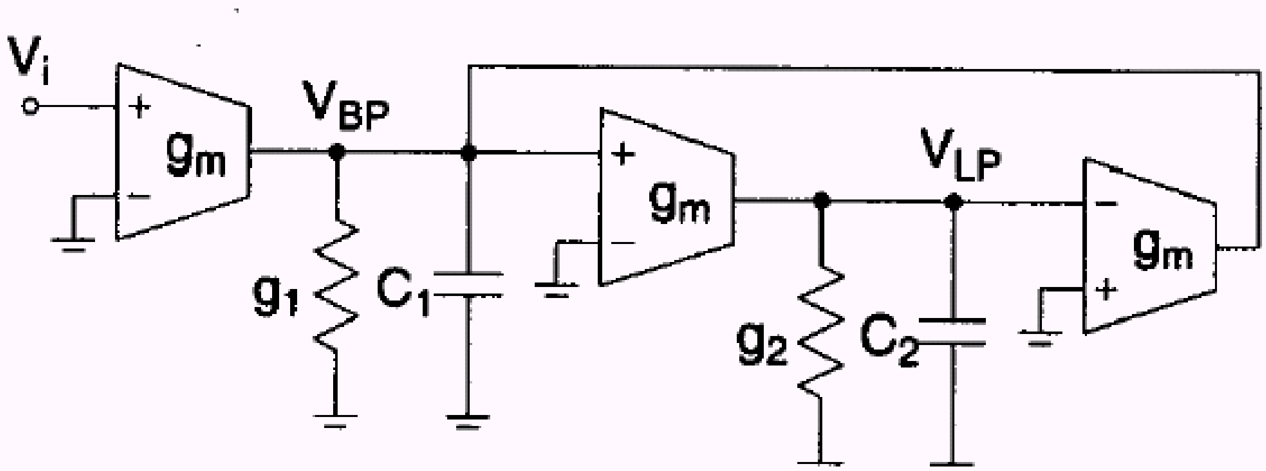
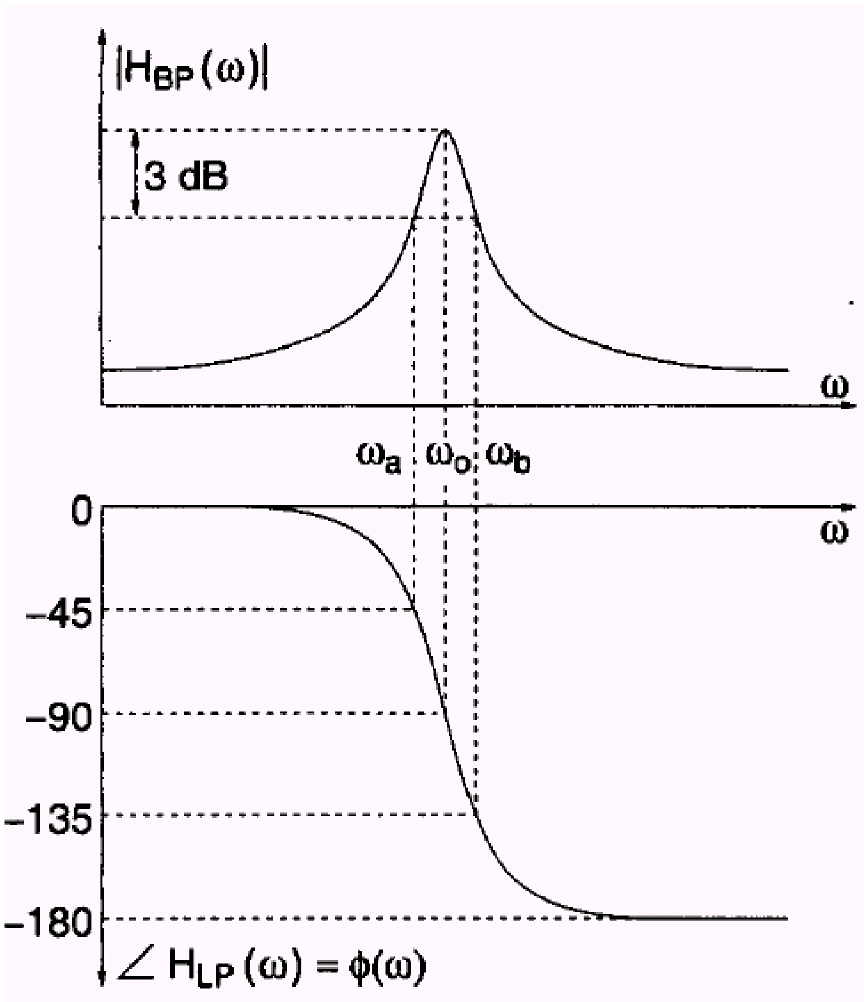


Figure 1: Second order $g_m - C$ filter.

$$H_{LP}(s) = \frac{\omega_o^2}{s^2 + s\omega_o/Q + \omega_o^2}$$

$$H_{BP}(s) = \frac{s\omega_o}{s^2 + s\omega_o/Q + \omega_o^2}$$

Tuning Circuit Technique: Phase Detect



Tuning Circuit Technique: Phase Detect

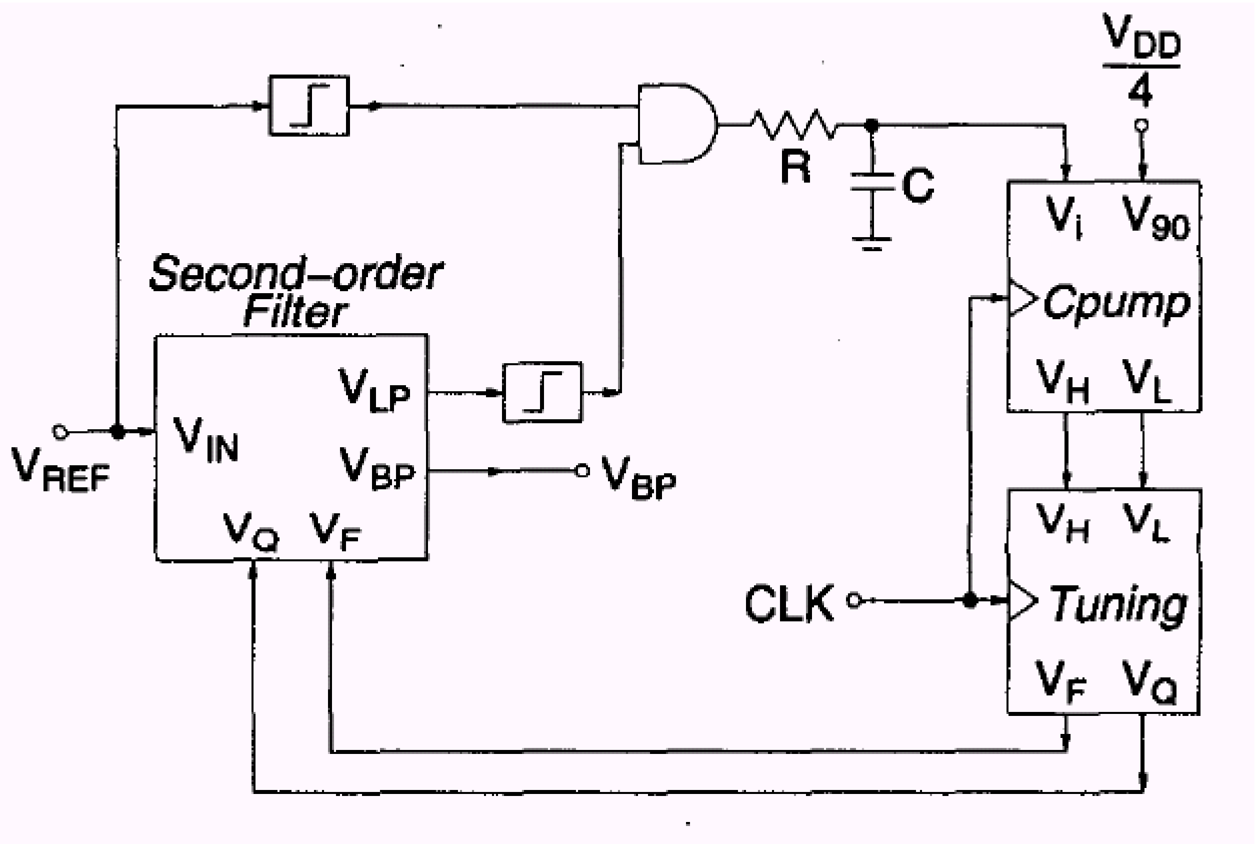


Figure 6: Complete tuning loop.

Tuning Circuit Technique: Peak Detect

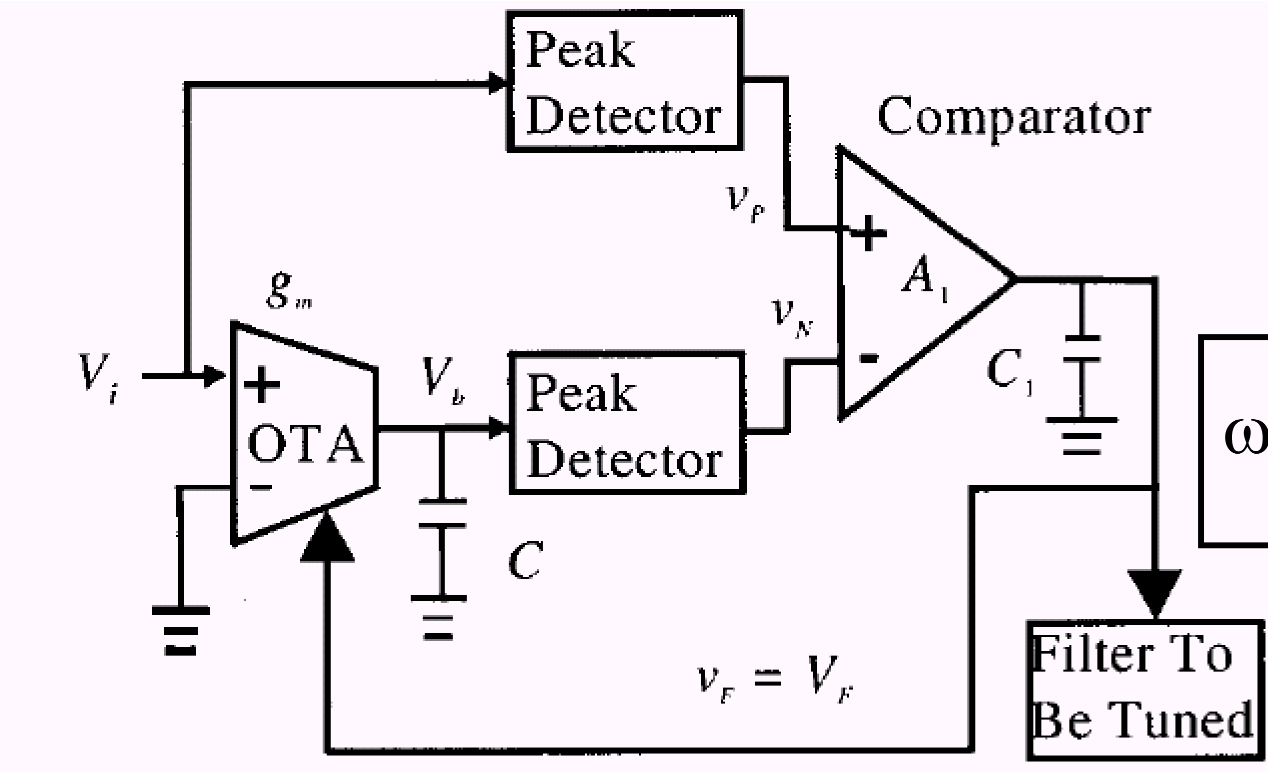
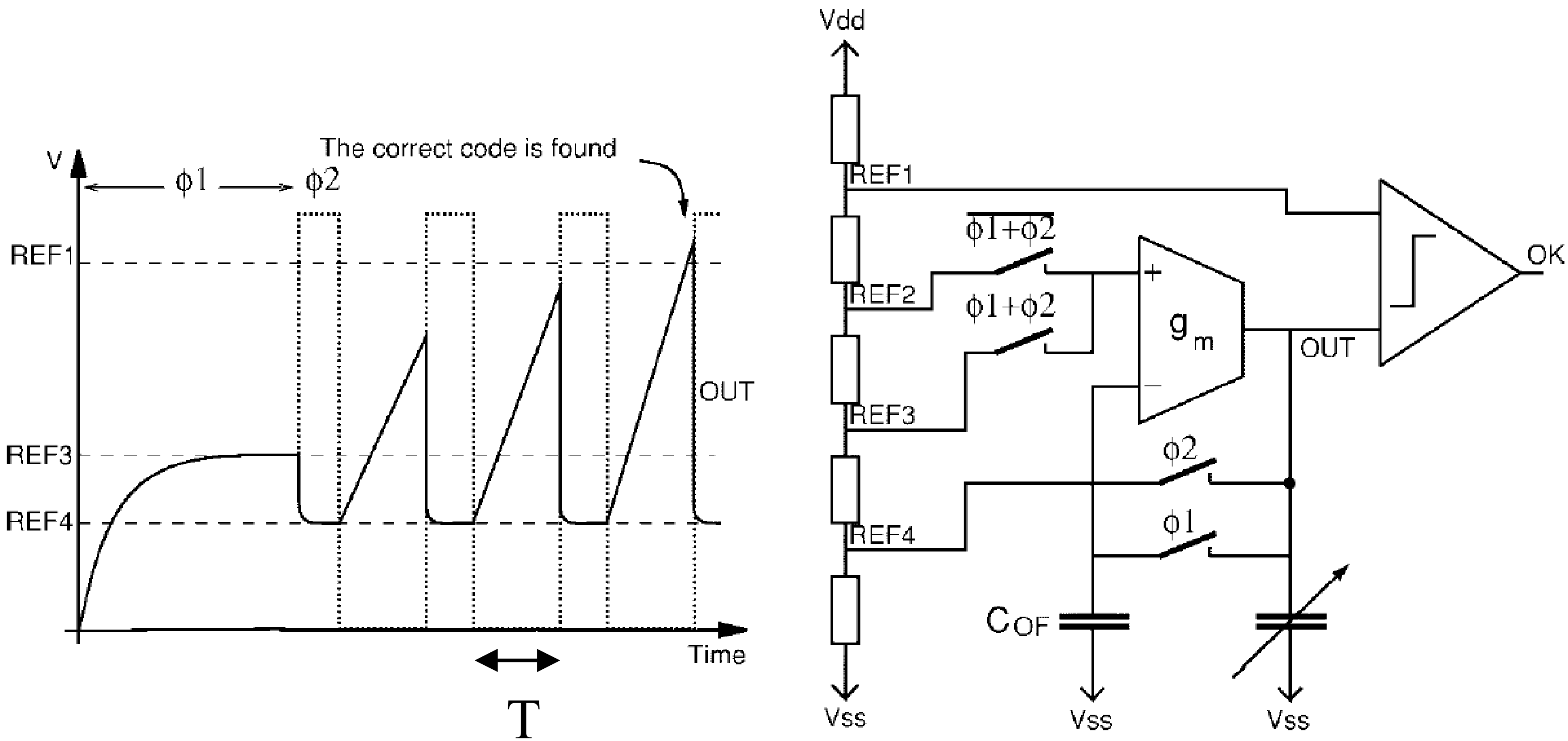


Figure 1 Block diagrams of frequency tuning scheme

$$\omega_{-3dB}\,\Big|_{Filter} = \frac{g_m}{C}\,\Big|_{dummy}$$

Tuning Circuit Technique: Linear Ramp(1)



$$\frac{g_m}{C} = \alpha \frac{1}{T}$$

Tuning Circuit Technique: Linear Ramp(2)