Spring 2002

# EEE598D: Analog Filter & Signal Processing Circuits

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Today: Introduction to SC Circuits

- SC Circuit Fundamental
- Charge Redistribution Analysis
- Transfer Function

# Introduction

- A SC circuit operates as a DT signal processor.
- Most easily analyzed using the z-transform.
- Require anti-aliasing and smoothing filters.
- The technique has become extremely popular due to:
  - Accurate frequency response (determined by capacitance ratios that can be set with an accuracy of 0.1% or better)
  - Good linearity and dynamic range
- Applications:
  - Filters, gain-stages, oscillators and modulators.

# Switched-Capacitor Fundamentals

- A switched capacitor simulates a resistor

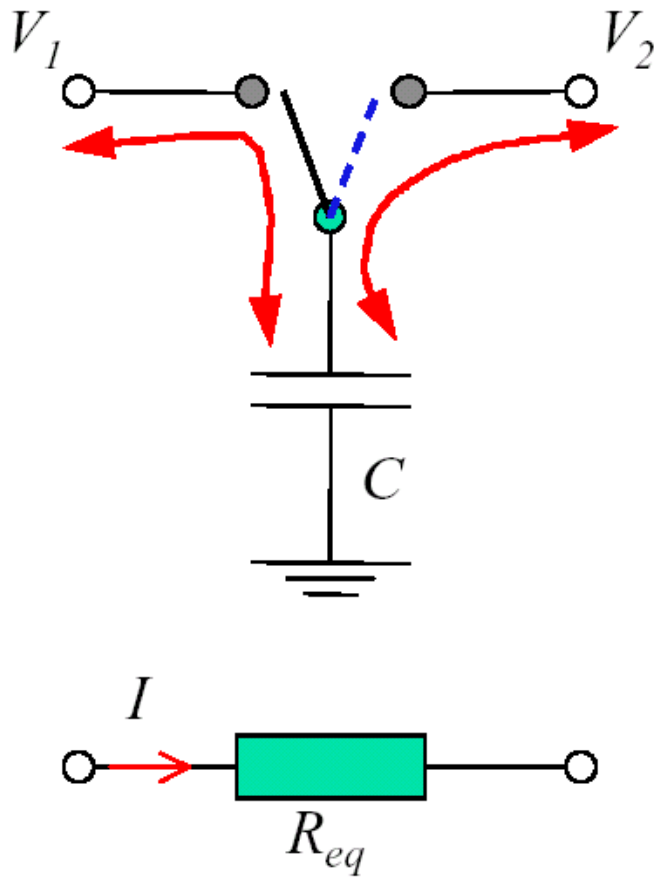
$$q(t) = C \cdot V_1$$

$$q(t+\tau) = C \cdot V_2$$

$$\Delta q(t) = C \cdot (V_1 - V_2)$$

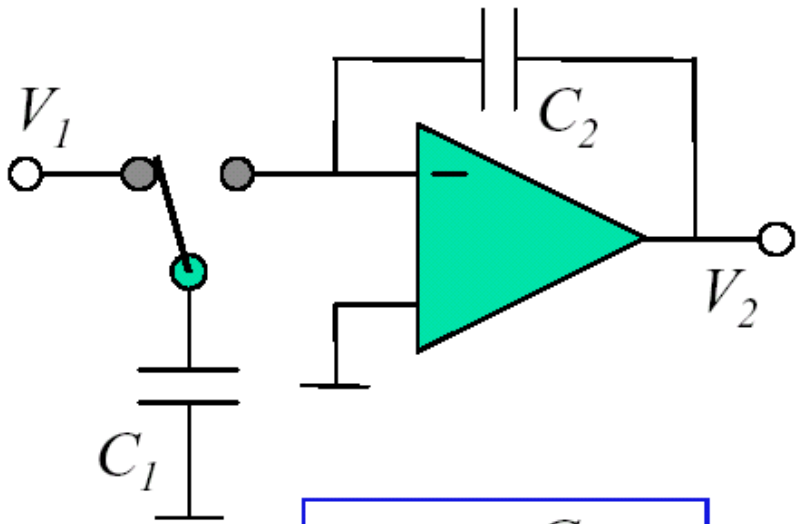
$$I = \Delta q(t)/T = C \cdot (V_1 - V_2)/T$$

$$R_{eq} = T/C$$



# First (Poor) SC Integrator

- Use the active-RC integrator and replace the resistor with a switched capacitor
- Capacitor ratio determines the transfer function
  - Improved matching
  - Low power possible



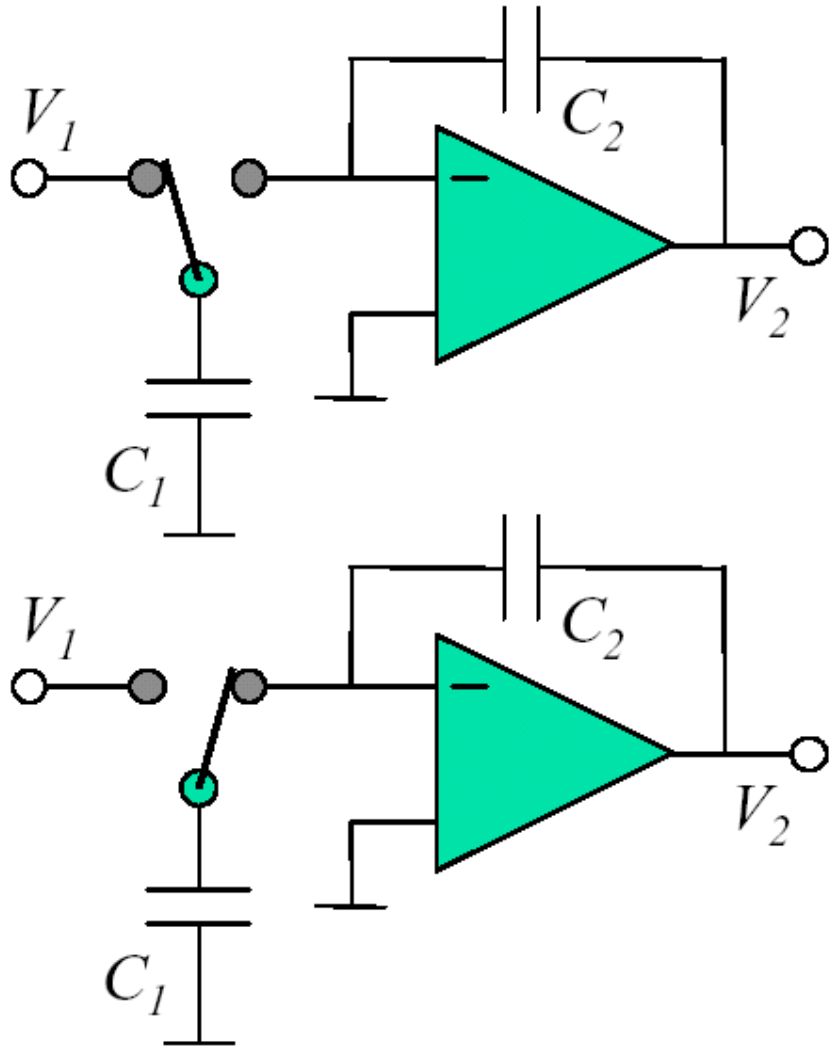

$$V_2 = -\frac{C_1}{sTC_2}V_1$$

# Charge Redistribution Analysis

- Consider the charge transportation
- OP outputs can take/give charge
- OP (CMOS) inputs cannot take/give charge
- Equilibrium will take place after settling
- No charge can disappear from an unconnected capacitor plate
- A capacitor with both plates connected to same potential will lose all of its charge

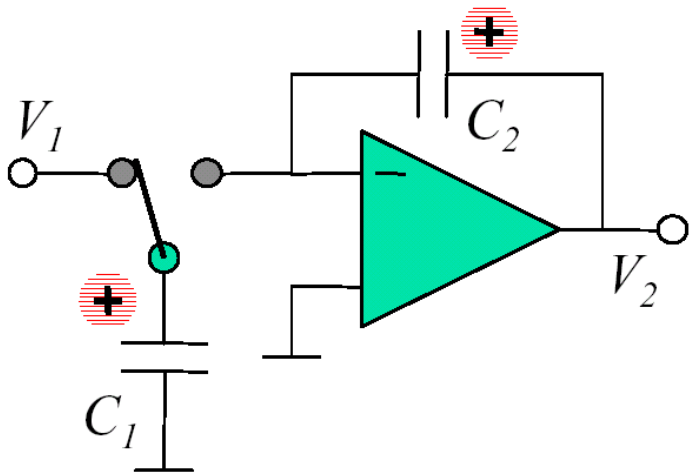
# Charge Redistribution Analysis

- Investigate both clock phases and denote the initial conditions in each phase
- Investigate the charge conservation and find the transfer function



# Charge Redistribution Analysis

- At t = t

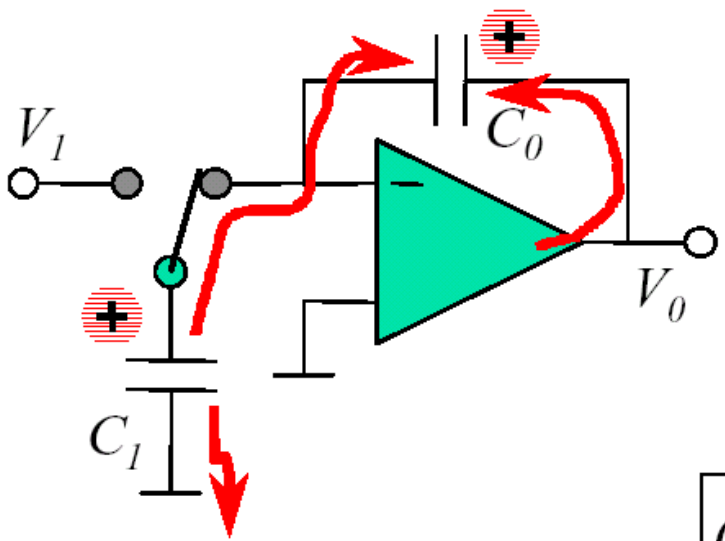



$$q_1(t) = C_1 \cdot V_1(t)$$
$$q_2(t) = C_2 \cdot V_2(t)$$

Denote references on the capacitors

# Charge Redistribution Analysis

- At t = t+T/2




$$q_1(t+\tfrac{T}{2}) = 0$$

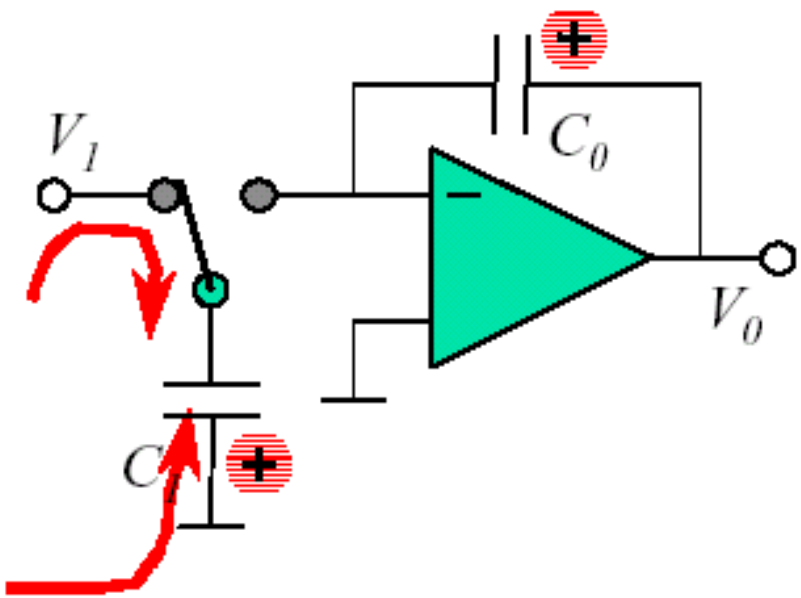
$$q_2(t+\tfrac{T}{2}) = C_2 \cdot V_2(t+\tfrac{T}{2})$$

$$\boxed{q_2(t+\tfrac{T}{2}) = -q_1(t) + q_2(t)}$$

- CI loses its charge to ground and C0

# Charge Redistribution Analysis

- At t = t+T




$$q_1(t+T) = C_1 \cdot V_1(t+T)$$

$$q_2(t+T) = C_2 \cdot V_2(t+T)$$

$$\boxed{q_2(t+T) = q_2(t+\tfrac{T}{2})}$$

- Charge conservation.

# Transfer Function

$$q_2(t+T) = q_2(t+\tfrac{T}{2}) = -q_1(t) + q_2(t)$$

$$C_2 \cdot V_2(t+T) = C_2 \cdot V_2(t) - C_1 \cdot V_1(t)$$

$$C_2 \cdot V_2(z) \cdot z = C_2 \cdot V_2(z) - C_1 \cdot V_1(z) \Rightarrow$$

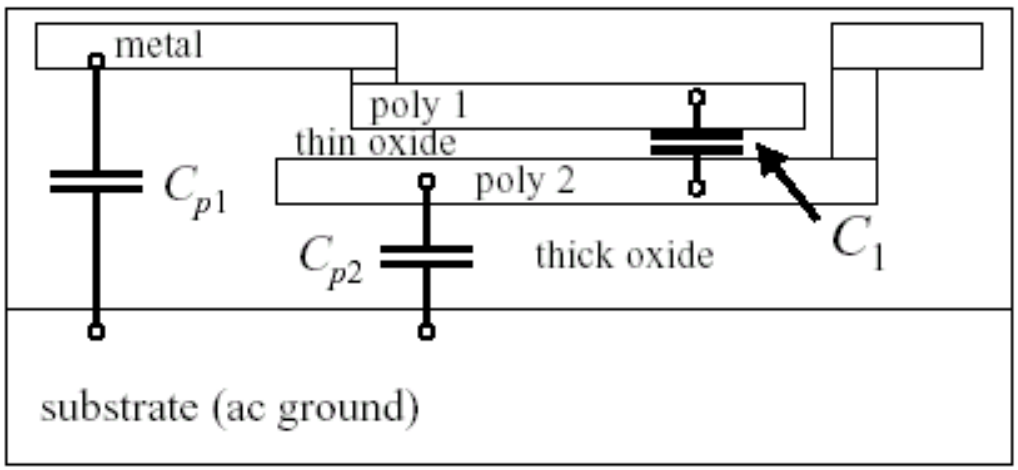
$$C_2 \cdot V_2(z) \cdot (z-1) = -C_1 \cdot V_1(z) \Rightarrow$$

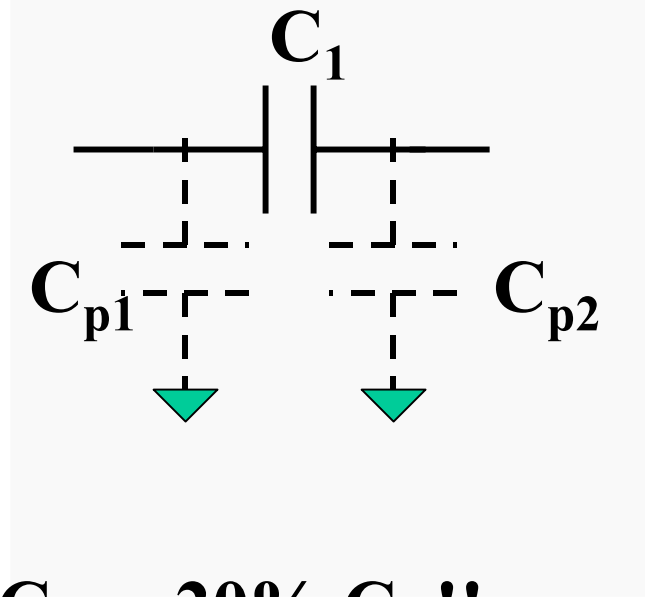
$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1}{C_2} \cdot \frac{1}{z-1} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}}$$

Inverting Discrete-time Integrator

# Influence of Parasitic Capacitors

- Parasitic from fringing capacitors and bottom-plate to substrate

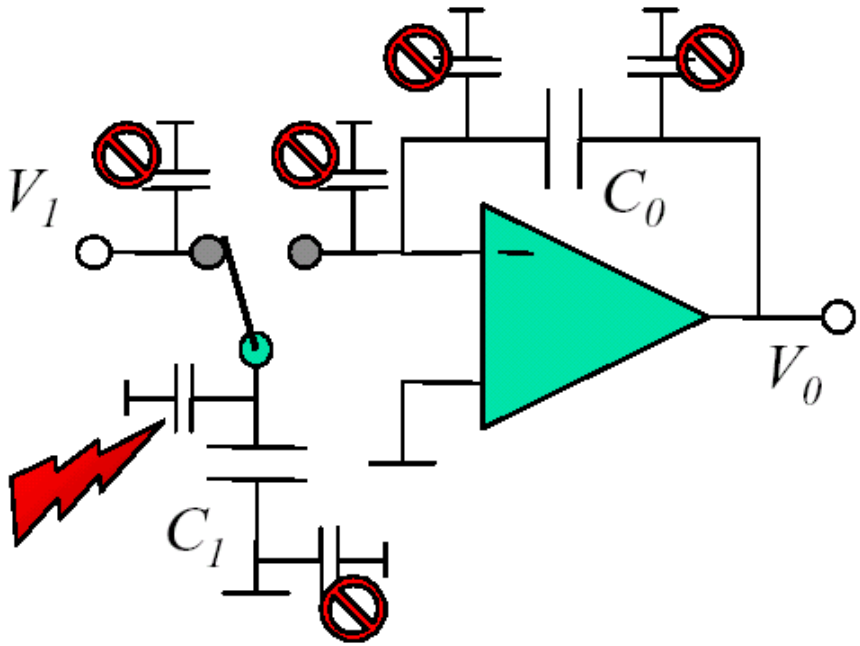



**$C_{p2} \sim 20\%\ C_1$ !!**

# Parasitic Capacitance

- Include parasitic to all capacitors, switches, etc.
- Remove those who do not effect the transfer function



# Transfer Function

$$q_2(t+T) = q_2(t+\tfrac{T}{2}) = -q_1(t) + q_2(t)$$

$$C_2 \cdot V_2(t+T) = -C_2 \cdot V_2(t) + (C_1 + C_P) \cdot V_1(t)$$

$$C_2 \cdot V_2(z) \cdot z = C_2 \cdot V_2(z) - (C_1 + C_P) \cdot V_1(z) \Rightarrow$$

$$C_2 \cdot V_2(z) \cdot (z-1) = -(C_1 + C_P) \cdot V_1(z) \Rightarrow$$

$$H(z) = \frac{V_2(z)}{V_1(z)} = -\frac{C_1 + C_P}{C_2} \cdot \frac{1}{z-1} = -\frac{C_1 + C_P}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}$$

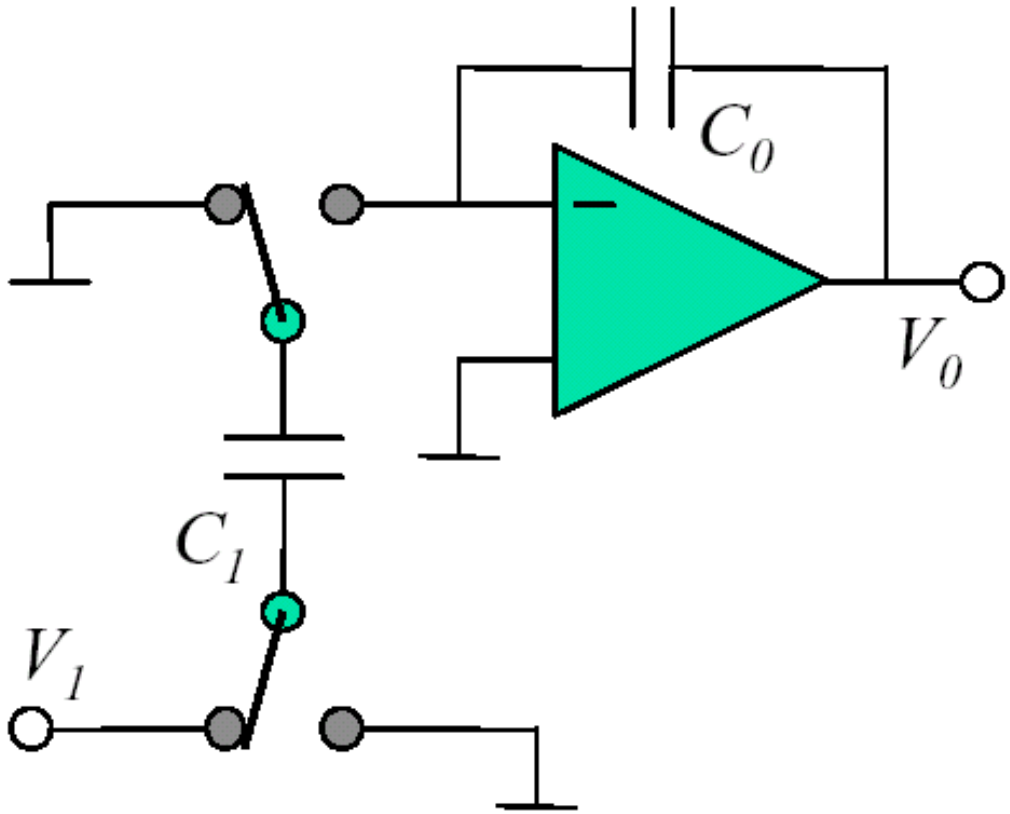
- Gain is affected by the parasitic.

# Parasitic Capacitors - Conclusions

Parasitic insensitive vs. sensitive

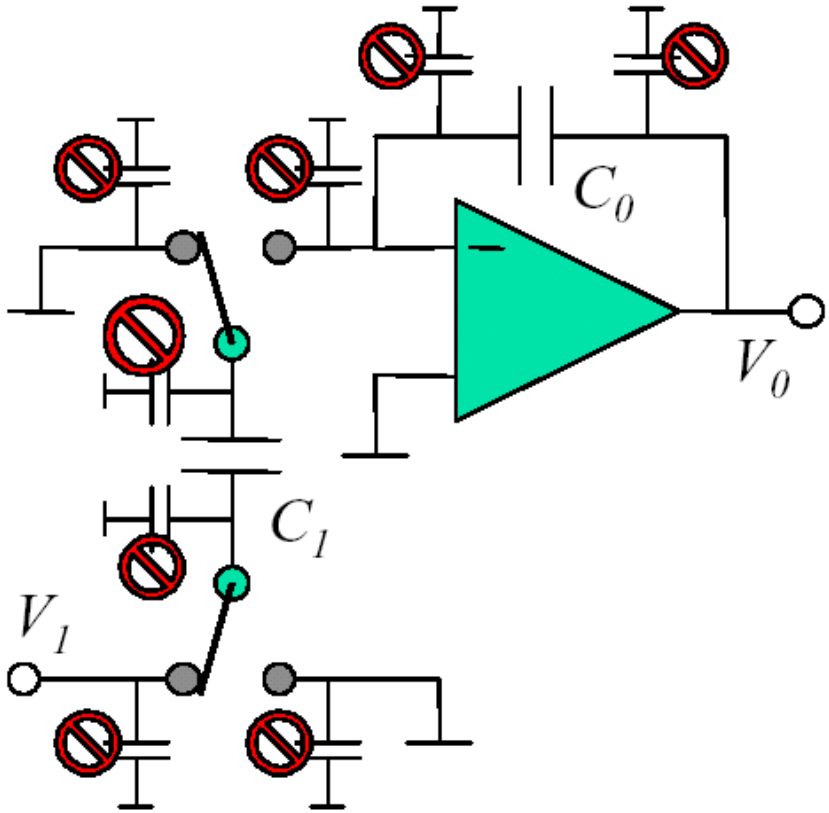
- To minimize the influence of parasitic:
  - Switch the capacitor between a voltage source and ground
  - Switch the capacitor between ground and virtual ground

# Parasitic Insensitive SC Circuits



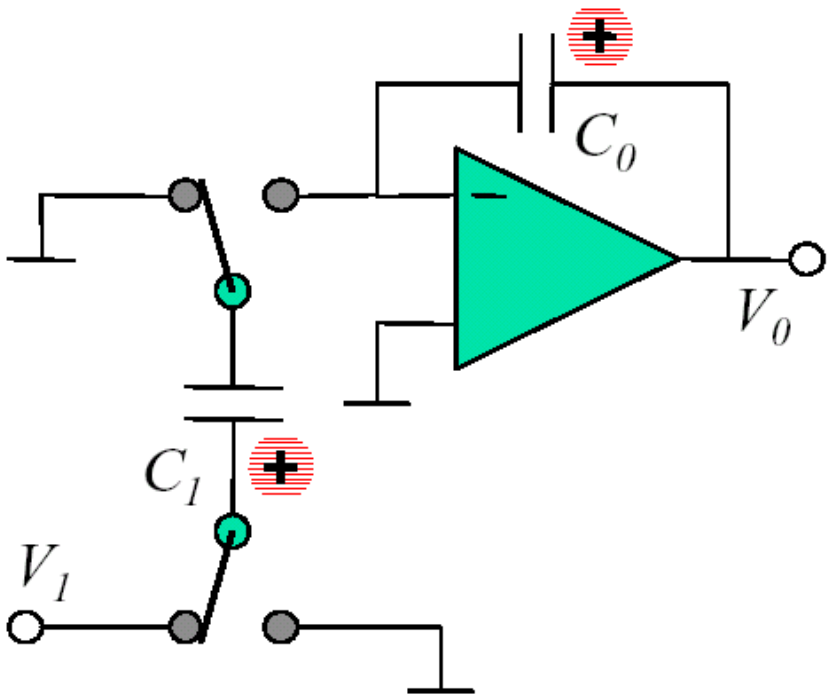
# Parasitic Insensitive SC Circuits

- Include parasitic to all capacitors, switches, etc.
- Remove those who do not effect the transfer function.



# Charge Redistribution Analysis

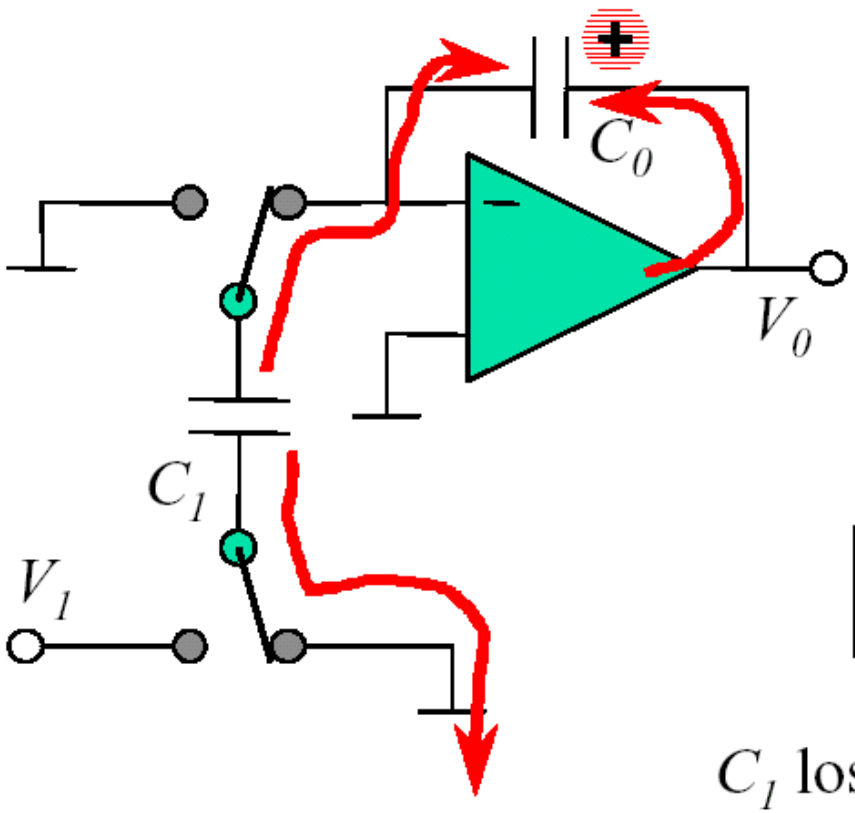
- At t = t




$$q_1(t) = C_1 \cdot V_1(t)$$
$$q_2(t) = C_2 \cdot V_2(t)$$

# Charge Redistribution Analysis

- At t = t + T/2




$$q_1(t+\tfrac{T}{2}) = 0$$

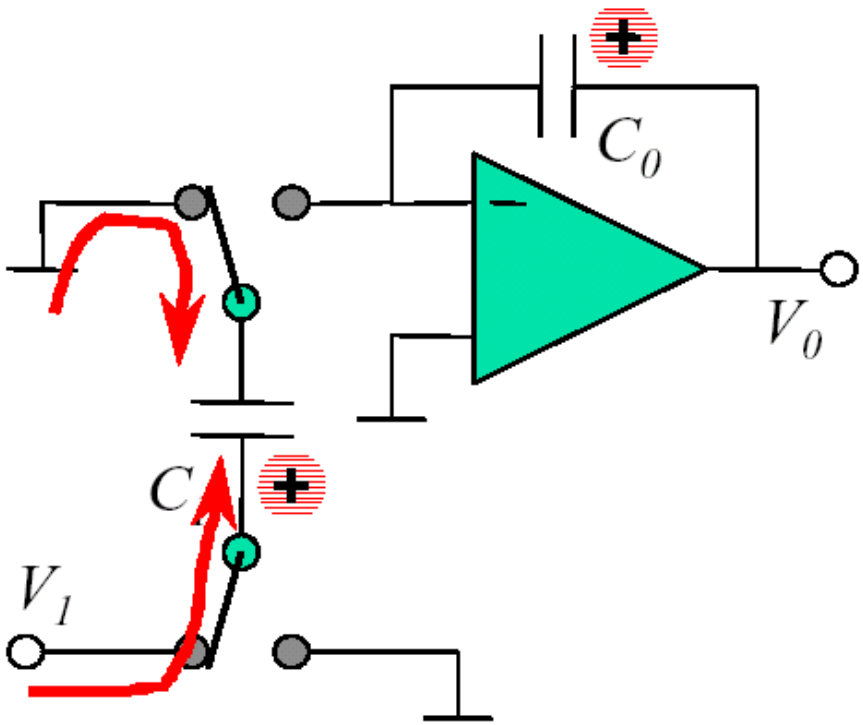
$$q_2(t+\tfrac{T}{2}) = C_2 \cdot V_2(t+\tfrac{T}{2})$$

$$\boxed{q_2(t+\tfrac{T}{2}) = q_1(t) + q_2(t)}$$

$C_1$ loses its charge to ground and $C_2$.

# Charge Redistribution Analysis

- At t = t + T




$$q_1(t+T) = C_1 \cdot V_1(t+T)$$

$$q_2(t+T) = C_2 \cdot V_2(t+T)$$

$$\boxed{q_2(t+T) = q_2(t+\tfrac{T}{2})}$$

Charge conservation

# Transfer Function

$$q_2(t+T) = q_2(t+\tfrac{T}{2}) = q_1(t) + q_2(t)$$

$$C_2 \cdot V_2(t+T) = C_2 \cdot V_2(t) + C_1 \cdot V_1(t)$$

$$C_2 \cdot V_2(z) \cdot z = C_2 \cdot V_2(z) + C_1 \cdot V_1(z) \Rightarrow$$

$$C_2 \cdot V_2(z) \cdot (z-1) = C_1 \cdot V_1(z) \Rightarrow$$

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2} \cdot \frac{1}{z-1} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1-z^{-1}}$$

Discrete-time Integrator

# Parasitic Capacitors Impact On Speed

- Both clock phases have to be investigated!
- Parasitic may influence the speed although the transfer function is not effected.
- Consider the feedback factor in each phase.

*(Feedback factor, $\beta$, is the amount of output signal fed back to the input, typically voltage divider).*

# Parasitic Capacitors Impact On Speed

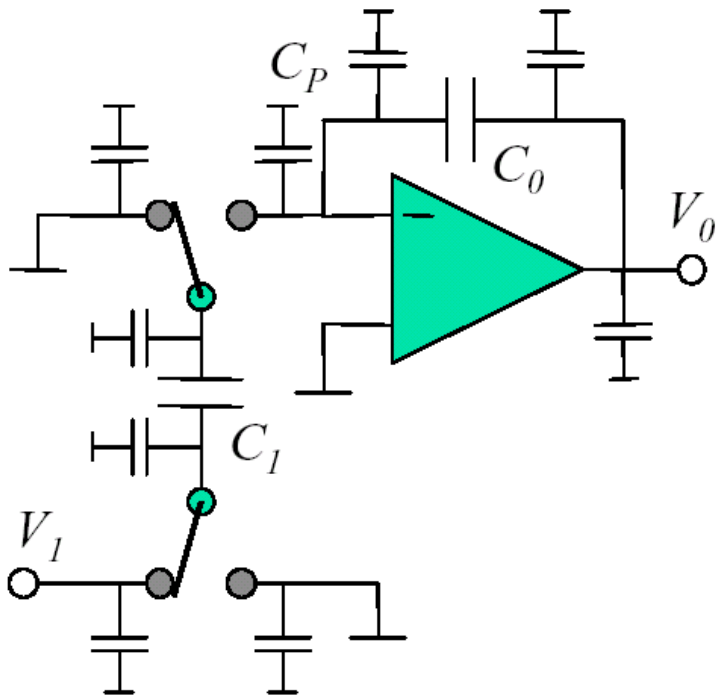
Phase 1

- The parasitic affect the load capacitance

$$\beta = \frac{C_0}{C_0 + C_{P1}}$$

$$\omega_{-3dB} = \beta \cdot \omega_u = \frac{C_0 \cdot \omega_u}{C_0 + C_{P1}}$$

$$\tau = 1 / \omega_{-3dB}$$



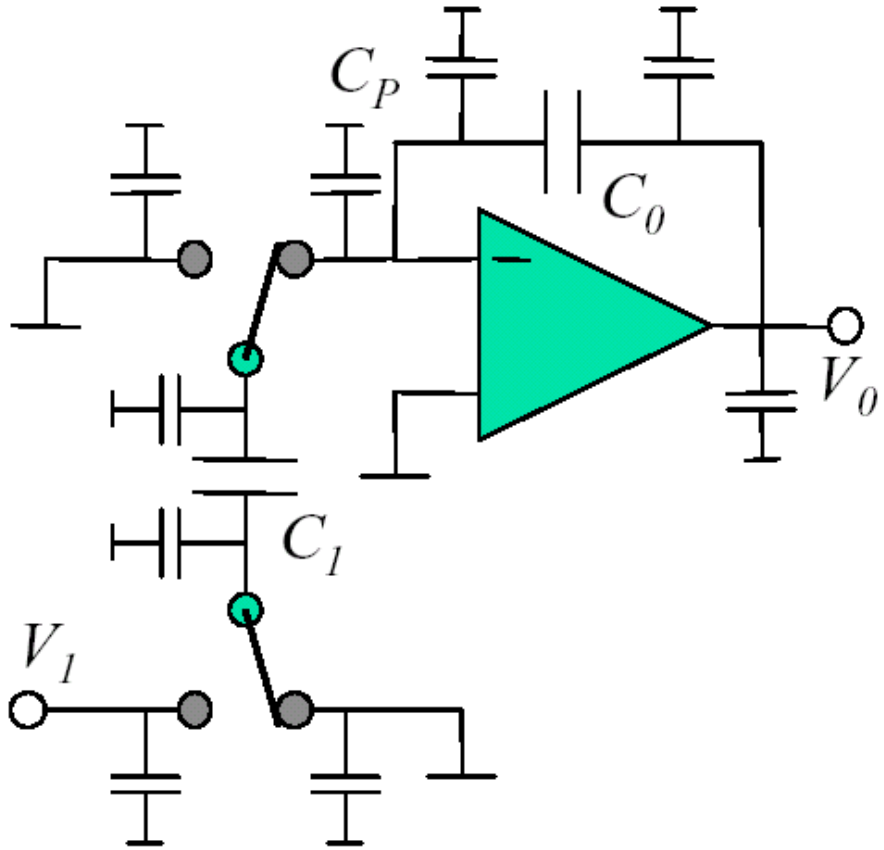
# Parasitic Capacitors Impact On Speed

## Phase 2

- Phase 2 is slower!

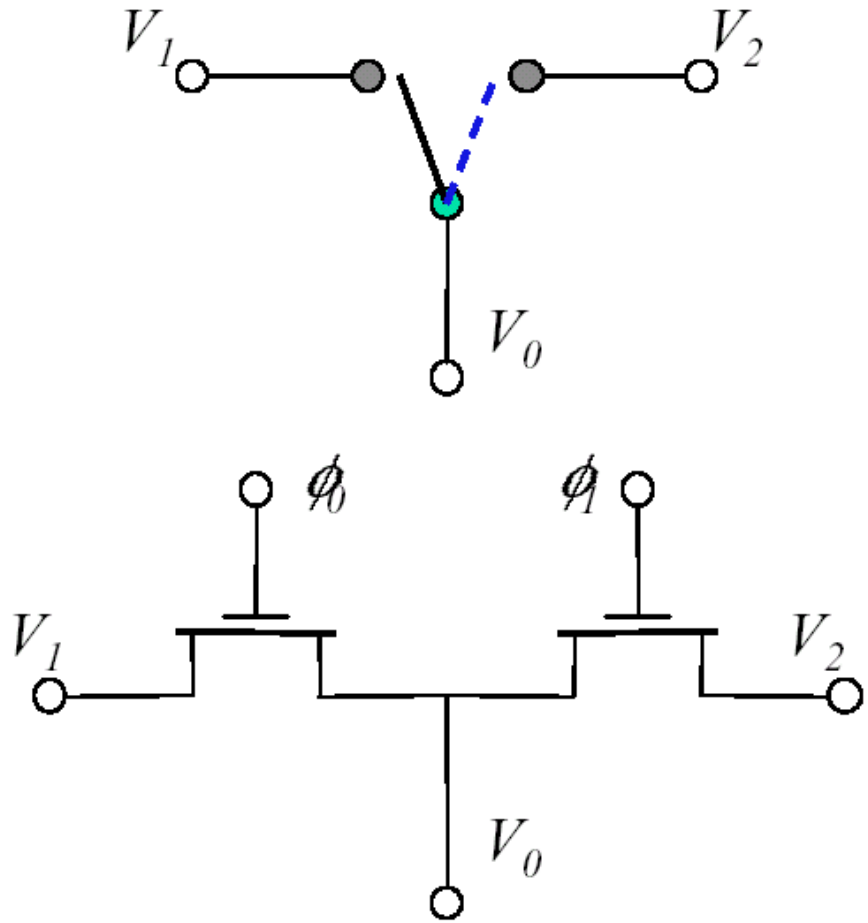
$$\beta = \frac{C_0}{C_0 + (C_{P2} + C_1)}$$

$$\omega_{-3dB} = \frac{C_0 \cdot \omega_u}{C_0 + (C_{P2} + C_1)}$$



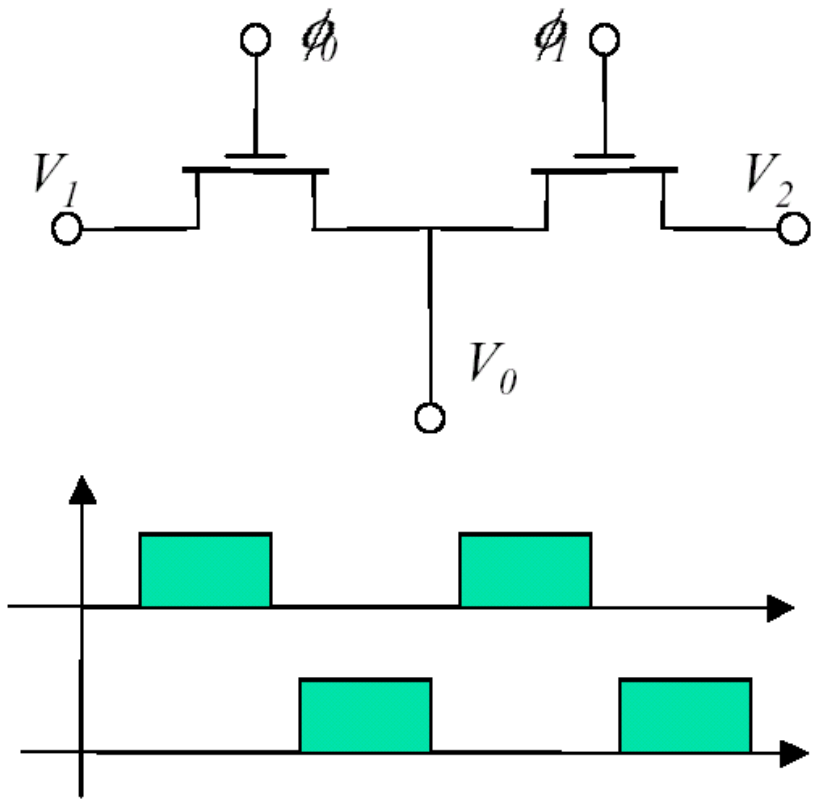
# Switches in SC Circuits

- Realized with NMOS transistors
  - To increase speed
  - To reduce size
  - RC-timing!



# Switches In SC Circuits

- Non-overlapping clock-phases
  - Guarantee that the two NMOS transistors, cannot conduct at the,same time
  - Reduces charge leakage

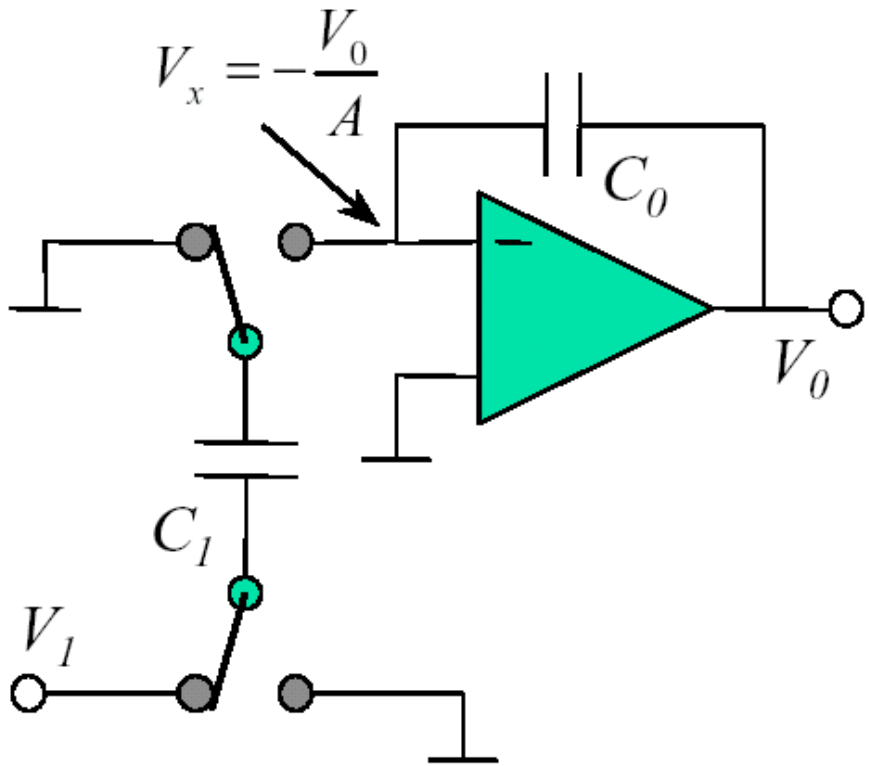


# Switches In SC Circuits

- Clock Feedthrough (CFT)
  - CFT affects the transfer function
  - Use small MOS switches
  - CFT Cancellation Techniques
  - Channel charge injection

# Influence of Non-Ideal OP

- Finite gain.
  - Assume the OP has a finite gain, A, (as in the real world)



# Influence of Finite Gain OP

$$\begin{cases} q_1(t) = C_1 \cdot V_1(t) \\ q_2(t) = C_2 \cdot (V_2(t) - (-V_2(t) \cdot \frac{1}{A}) \end{cases}$$

$$\begin{cases} q_1(t+\frac{T}{2}) = -C_1 \cdot (-V_2(t+\frac{T}{2}) \cdot \frac{1}{A}) \\ q_2(t+\frac{T}{2}) = C_2 \cdot V_2(t+\frac{T}{2}) \cdot (1+\frac{1}{A}) \end{cases}$$

$$q_2(t+\tfrac{T}{2}) + q_1(t+\tfrac{T}{2}) = q_1(t) + q_2(t)$$

$$q_2(t+T) = q_2(t+\tfrac{T}{2}) \Rightarrow V_2(t+\tfrac{T}{2}) = V_2(t)$$

$$C_2 \cdot V_2(t+T) \cdot (1+\tfrac{1}{A}) = C_1 \cdot V_1(t) + C_2 \cdot V_2(t) \cdot (1+\tfrac{1}{A}) - C_1 \cdot V_2(t+T) \cdot \tfrac{1}{A}$$

# Influence of Finite Gain OP

$$C_2 \cdot V_2(z) \cdot z \cdot (1+\tfrac{1}{A}) = C_1 \cdot V_1(z) + C_2 \cdot V_2(z) \cdot (1+\tfrac{1}{A}) - C_1 \cdot V_2(z) \cdot z \cdot \tfrac{1}{A}$$

$$V_2(z) \cdot (C_2 \cdot z \cdot (1+\tfrac{1}{A}) - C_2 \cdot (1+\tfrac{1}{A}) - C_1 \cdot z \cdot \tfrac{1}{A}) = C_1 \cdot V_1(z)$$

$$H(z) = \frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_2} \cdot \frac{1}{z + \frac{1}{1+\frac{C_1/C_2}{1+A}}} \cdot \frac{1}{1+(1+\frac{C_1}{C_2}) \cdot \frac{1}{A}}$$

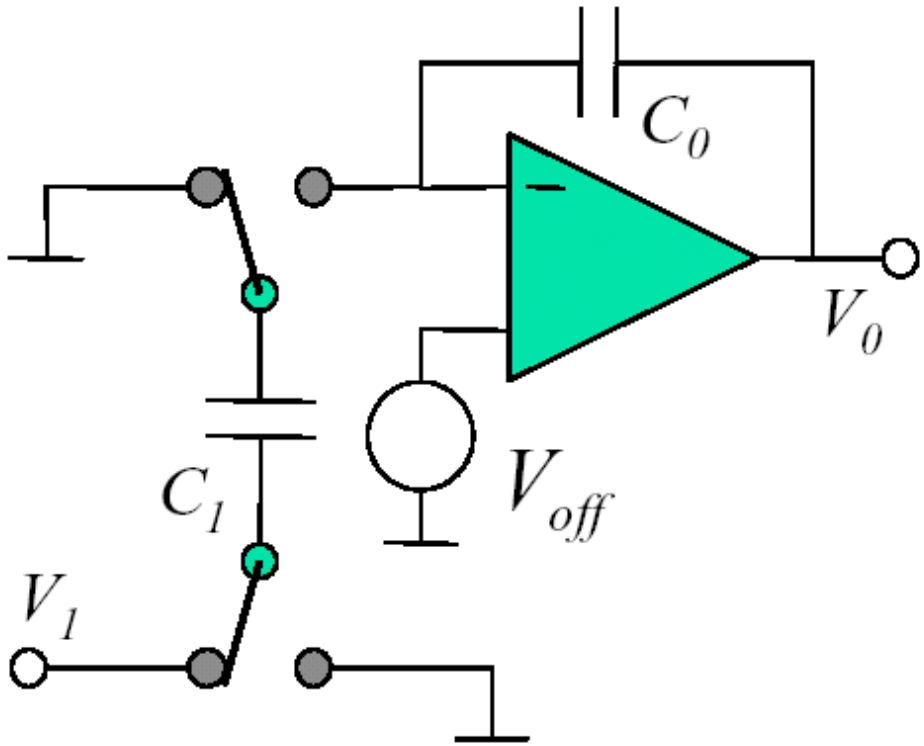
The pole is moved

The gain is changed

- Lossy Integrator!

# Influence of OP Offset Voltage

- Input offset voltage.
  - Matching errors can be modeled as a voltage source, Voff, at the input of the OP.



# Influence of OP Offset Voltage

$$\begin{cases} q_1(t) = C_1 \cdot V_1(t) \\ q_2(t) = C_2 \cdot (V_2(t) - V_{off}) \end{cases}$$

$$\begin{cases} q_1(t+\frac{T}{2}) = -C_1 \cdot V_{off} \\ q_2(t+\frac{T}{2}) = C_2 \cdot (V_2(t+\frac{T}{2}) \cdot V_{off}) \end{cases}$$

$$q_2(t+\tfrac{T}{2}) + q_1(t+\tfrac{T}{2}) = q_1(t) + q_2(t)$$

$$q_2(t+T) = q_2(t+\tfrac{T}{2}) \Rightarrow V_2(t+\tfrac{T}{2}) = V_2(t)$$

$$C_2 \cdot (V_2(t+T) - V_{off}) = C_1 \cdot V_1(t) + C_2 \cdot (V_2(t) - V_{off}) + C_1 \cdot V_{off}$$

$$C_2 \cdot V_2(t+T) = C_1 \cdot V_1(t) + C_2 \cdot V_2(t) + C_1 \cdot V_{off}$$

# Influence of OP Offset Voltage

$$C_2 \cdot V_2(z) \cdot z = C_1 \cdot V_1(z) + C_2 \cdot V_2(z) + C_1 \cdot V_{off}$$

$$V_2(z) = \frac{C_1}{C_2} \cdot \frac{1}{z-1} \cdot V_1(z) + \frac{C_1}{C_2} \cdot \frac{1}{z-1} \cdot V_{off}$$

Offset voltage is accumulated

- We need an SC circuit with offset compensation technique. That circuit must have a so called auto-zeroing phase.