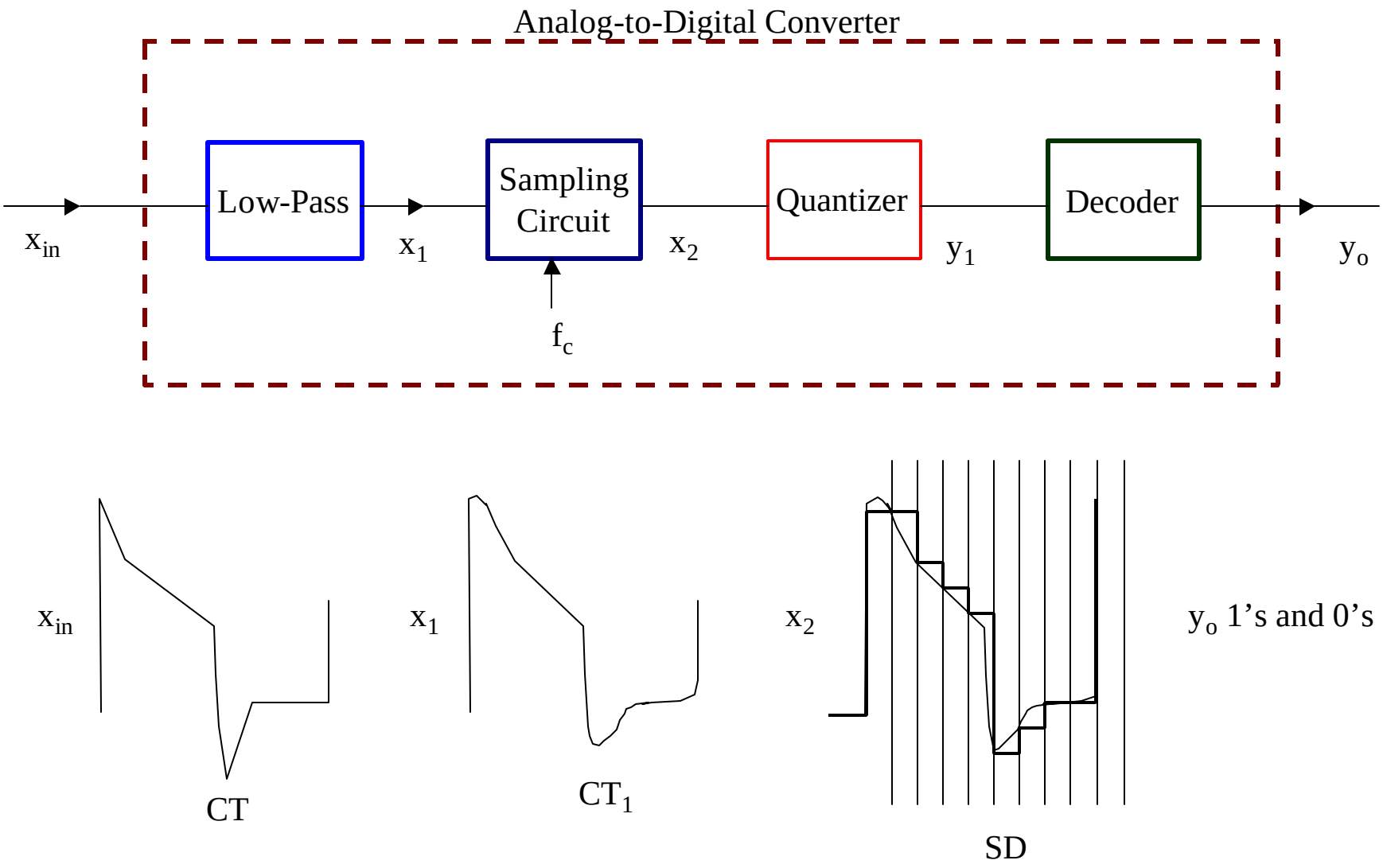
Switched-Capacitor Circuits

- Mathematical Background
- Basic Building Blocks
- SC Filters
- SC Oscillators
- SC PLL

Examples of Analog and Digital Signals



Analog and Digital Signals and Systems Concepts

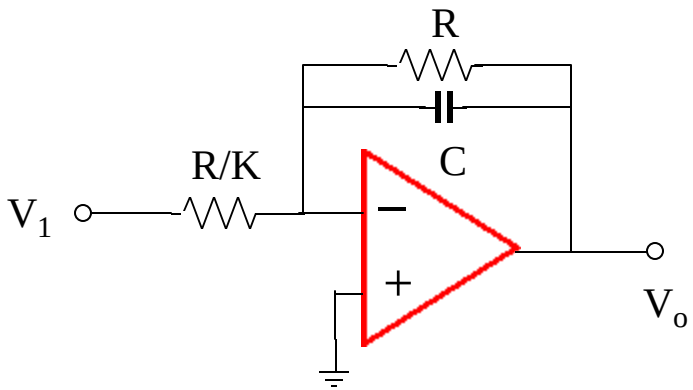
Types of signals	Mathematical Description
• Continuous-Time (CT) --Continuous values in time --Continuous values in magnitude	Laplace
• Sampled Data (SD) --Continuous values in magnitude --Discrete values in time	Z-Transform
• Digital --Discrete values in magnitude --Discrete values in time	Z-Transform

Examples of Basic Implementations

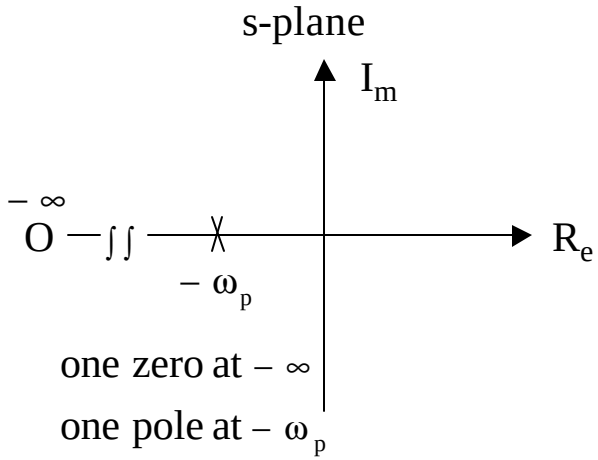
- First-order Low Pass (Continuous-Time)

$$H(s) = \frac{K}{1 + s/\omega_p} \quad ; \quad \frac{V_o(s)}{V_{in}(s)} = \frac{K\omega_p}{s + \omega_p} \quad ; \quad \frac{dv_o(t)}{dt} + \omega_p v_o(t) = K\omega_p \, v_{in}(t)$$

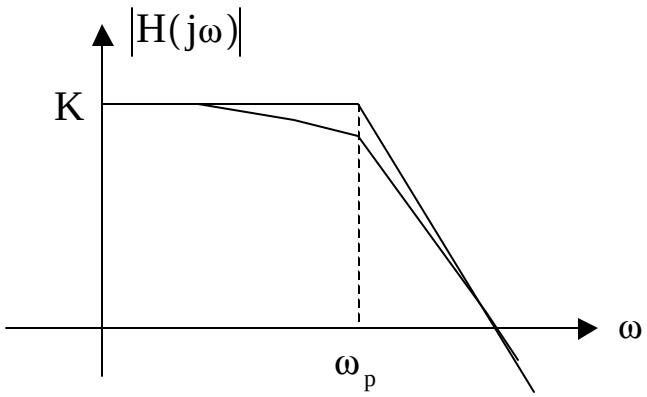
Continuous-time



$$C = \frac{1}{R\omega_p}$$

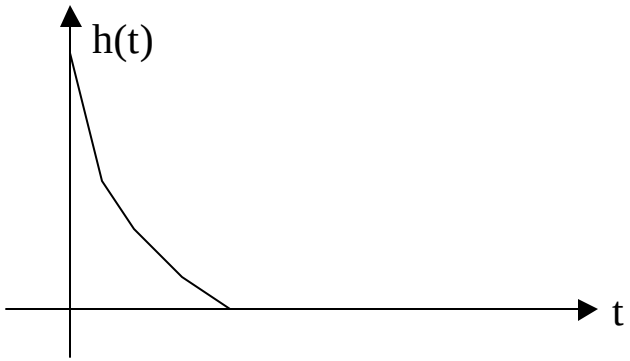


Stability implies to have poles in the left-half plane (LHP)



$$H(s)\Big|_{s=j\omega} = H(j\omega) = \frac{-K}{1+ j\omega/\omega_p} = \frac{K}{\left[1+(\omega/\omega_p)^2\right]^{1/2}} \angle -\tan \omega/\omega_p$$

Frequency Response

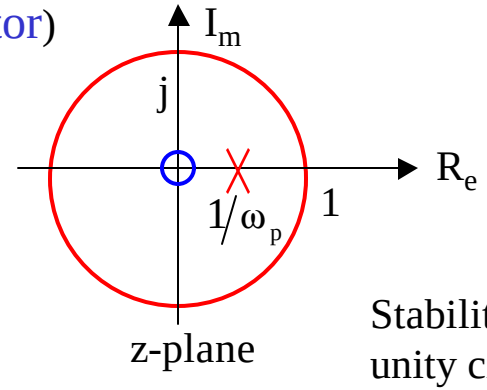


$$h(t) = K\omega_p e^{-\omega_p t}$$

Impulse Response

- First-Order Low-Pass (Discrete-Time) Sampled-Data (i.e., Switched-Capacitor)

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{K_1}{1 - z^{-1}/\omega_{p1}} = \frac{K_1\omega_{p1}}{\omega_{p1} - z^{-1}};$$



Stability implies poles inside unity circle

$$[\omega_{p1} - z^{-1}]V_o(z) = K_1\omega_{p1}V_{in}(z)$$

$$\omega_{p1}V_o(z) - z^{-1}V_o(z) = K_1\omega_{p1}V_{in}(z)$$

Taking the inverse z-transform

$$\omega_{p1}v_o(nT) - v_o(n-1)T = K_1\omega_{p1}v_{in}(nT)$$

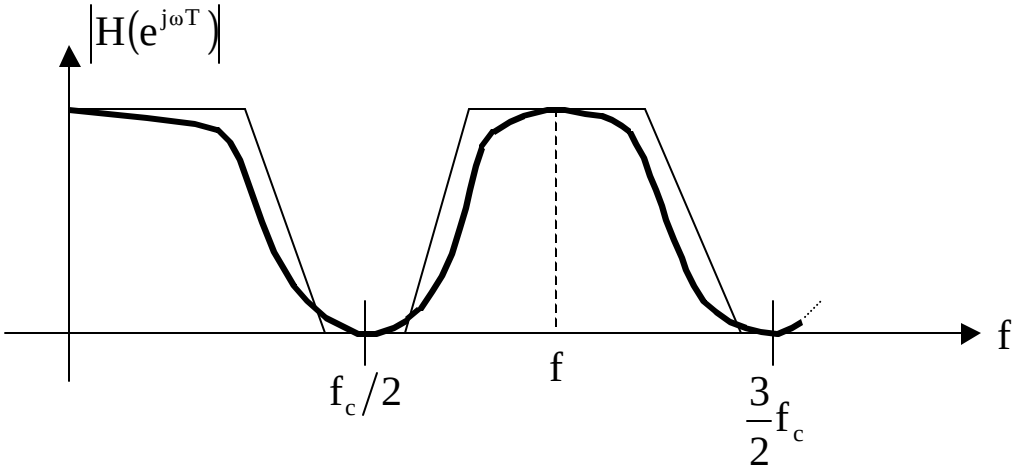
$$v_o(n-1)T - \omega_p v_o(nT) = -K_1\omega_{p1}v_{in}(nT)$$

This difference equation represents the first-order low pass in the Z-domain.

Note that

$$Z^{-1}X_o(z) \Rightarrow x_o(n-1)T$$

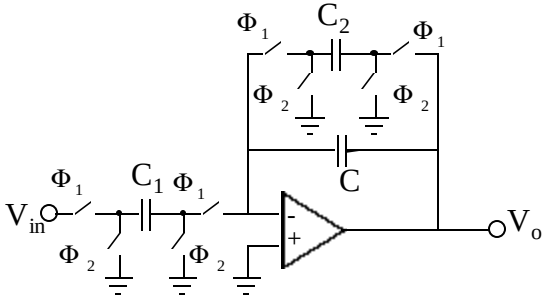
$$Z^{-b}X_o(z) \Rightarrow x_o(n-b)T$$



Frequency Response (A periodic transfer function!)

$$H(z) = \frac{K_1\omega_{p1}Z}{\omega_{p1}Z - 1}\Bigg|_{z = e^{j\omega}} = \frac{K_1\omega_{p1}(\cos\omega T + j\sin\omega T)}{(\omega_{p1}\cos\omega T - 1) + j\sin\omega T}$$

$$H(e^{j\omega}) = \frac{K_1\omega_{p1}}{\left\{(\omega_{p1}\cos\omega T - 1)^2 + \sin^2\omega T\right\}^{1/2}} \left[\overbrace{\omega T - \tan^{-1}\frac{\sin\omega T}{\omega_{p1}\cos\omega T - 1}}^{\text{phase}}\right]$$



where

$$K_1\omega_{p1} = \frac{C_1}{C}$$

$$\omega_{p1} = 1 + \frac{C_2}{C}$$

What are the relationships between the s-plane and z-plane?

- There are a number of mappings between the two planes
- The most popular and exact is the bilinear mapping.

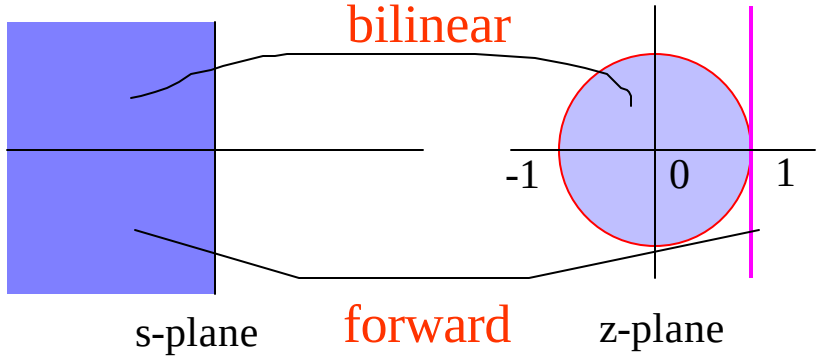
$$s = \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}} = \frac{2}{T}\frac{z - 1}{z + 1} \quad \text{or} \quad z = \frac{1 + (T/2)s}{1 - (T/2)s}$$

- The commonly used for high-sampling rate is:

$$s = \frac{1}{T}\frac{1 - z^{-1}}{z^{-1}} = \frac{1}{T}\frac{z - 1}{1}$$

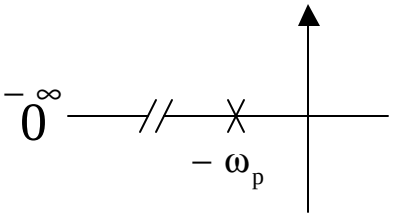
or

$$z = sT + 1$$

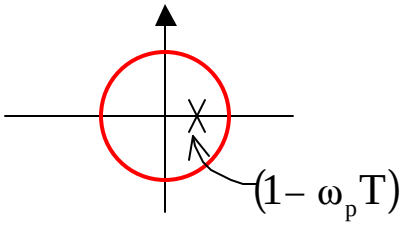


Example. Approximate a first-order low-pass continuous-time to a discrete-time low-pass under high-sampling conditions. $(fs/f \gg 1)$

$$H(s) = \frac{K}{1 + s/\omega_p} = \frac{K\omega_p}{s + \omega_p} \Bigg|_{s = \frac{1}{T}(z-1)}$$



$$H(z) = \frac{K\omega_p T}{z - 1 + \omega_p T} = \frac{K\omega_p T}{z - (1 - \omega_p T)}$$



What is the 3dB cut-off frequency in both domains?

$f_{3dB} = \omega_p$ CT

For H(z) is more complex than the computation of f_{3dB}.

$$H(e^{j\omega T}) = \frac{K\omega_p T}{\cos\omega T + j\sin\omega T - (1 - \omega_p T)}$$

$$\left|H(e^{j\omega T})\right| = \left|H(e^{j\omega_{3dB} T})\right|/\sqrt{2}$$

$$\omega = \omega_{3dB}$$

$$\omega_{3dB} = \frac{1}{T}\cos^{-1}\frac{2 - 2\omega_p T - (\omega_p T)^2}{2(1 - \omega_p T)}$$

Numerical example. Low-Pass (First Order)

$$\omega_p = 2\pi \times 10^3 \, r/s$$

$$f_c = f_s = 20KHz \quad ; \quad T = 1/f_s \quad ; \quad \omega_p T = \frac{2\pi \times 10^3}{20 \times 10^3} = 0.1\pi$$

$$K = 2$$

For the continuous-time

$$f_{3dB} = 1KHz$$

$$\left| H(j\omega) \right|_{\omega = \omega_{3dB}} = \frac{2}{\sqrt{2}} = 1.4142$$

For the sample-data

$$f_{3dB} = \frac{f_s}{2\pi} \cos^{-1} \frac{2 - 2\omega_p T - (\omega_p T)^2}{2(1 - \omega_p T)}$$

$$f_{3dB} \cong 1.16KHz$$

Switched - Capacitor Filters

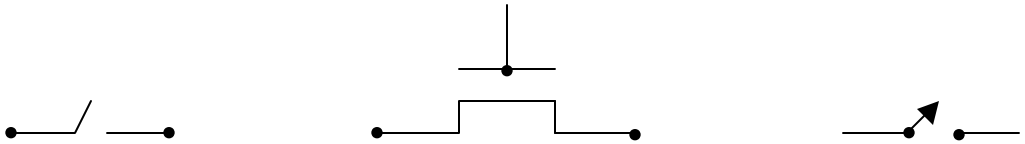
- Use Z-transform mathematics
- Are described by difference equations
- Time constants are proportional to capacitor ratios
- Best implementation for audio applications
- Originally the basic goal was to replace resistors by switches and capacitors
- This design approach is one of the most popular in the industry

Advantages

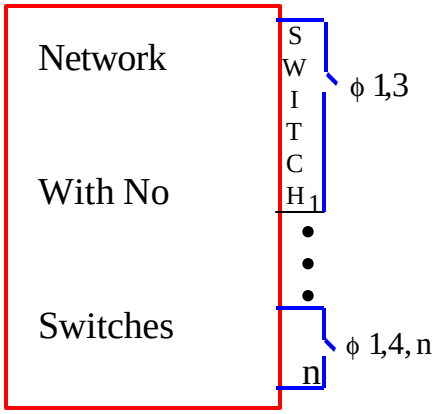
- Reduced silicon area
- Good accuracy. Time constants are implemented with capacitor ratios (~0.1%)
- Don’t require a low-impedance output stage (OTA’s could be used)
- Could be implemented using digital circuit process technology
- Very useful in the audio range

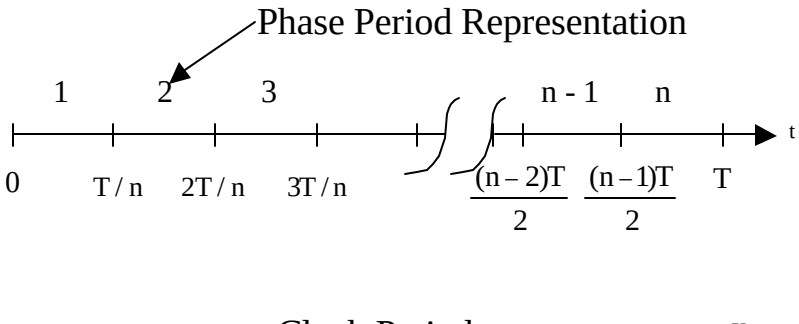
NOTATION

Switches



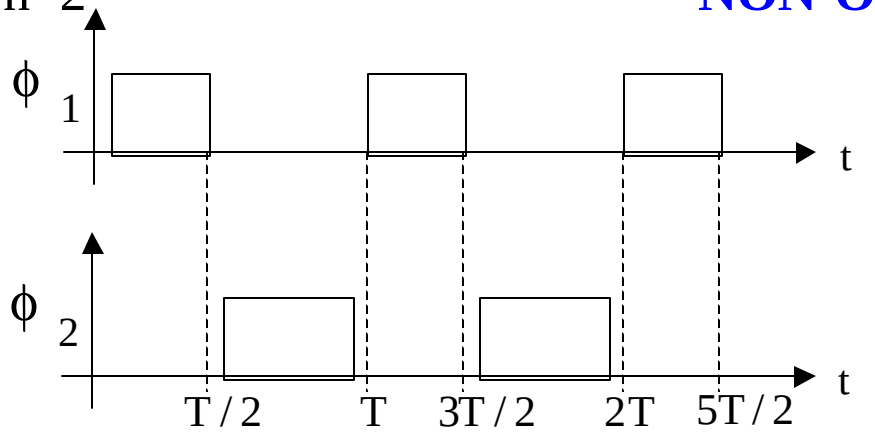
Representation



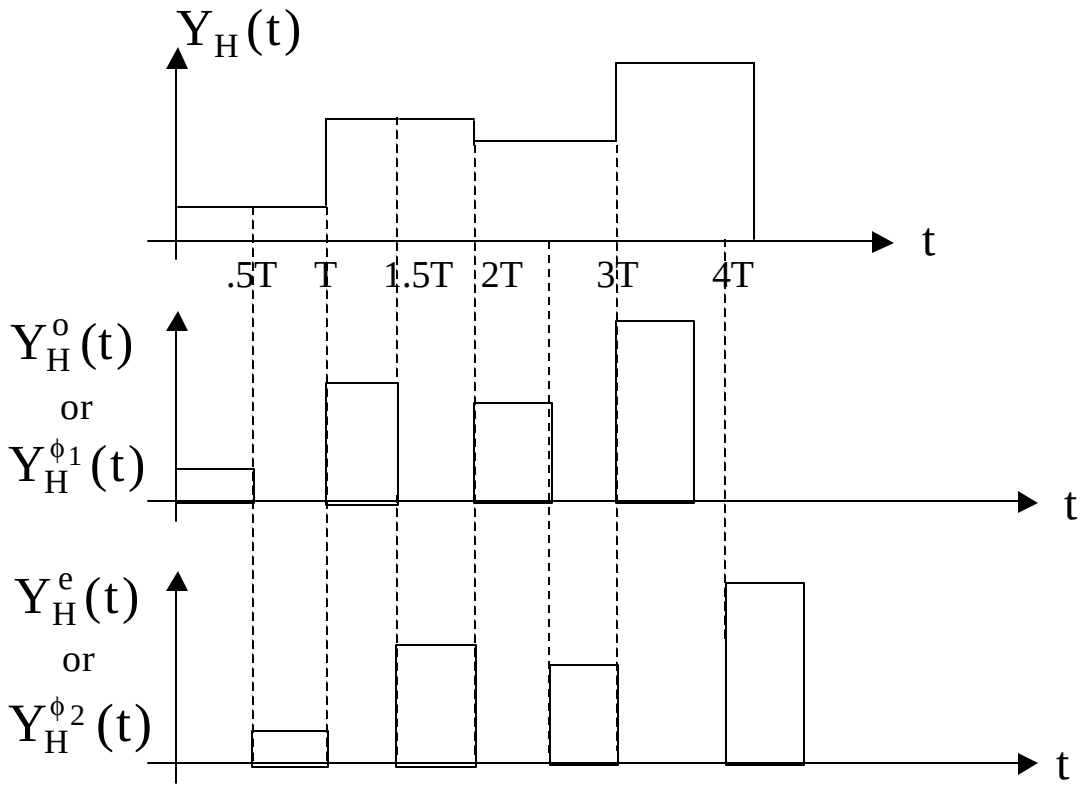


EXAMPLE n=2

NON-OVERLAPPING



PHASE PERIODS OF A CONVENTIONAL CLOCK SEQUENCE

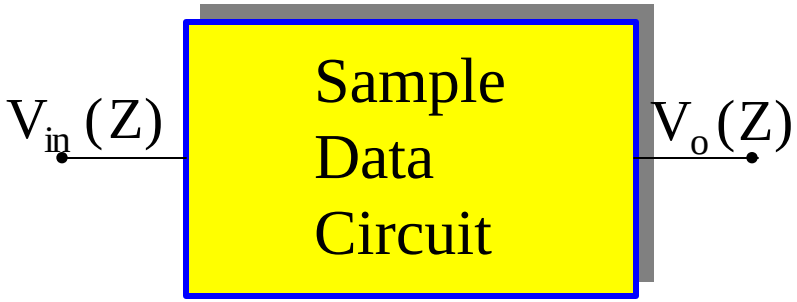


S/H and its respective odd and even components

$$y_H(t) = y_H^o(t) + y_H^e(t)$$

or

$$Y_H(Z) = Y_H^o(Z) + Y_H^e(Z)$$



$$V_{in}(Z) = V_{in}^{e}(Z) + V_{in}^{o}(Z)$$

$$V_o(Z) = V_o^{e}(Z) + V_o^{o}(Z)$$

$$H(Z) = \frac{V_o(Z)}{V_{in}(Z)}$$

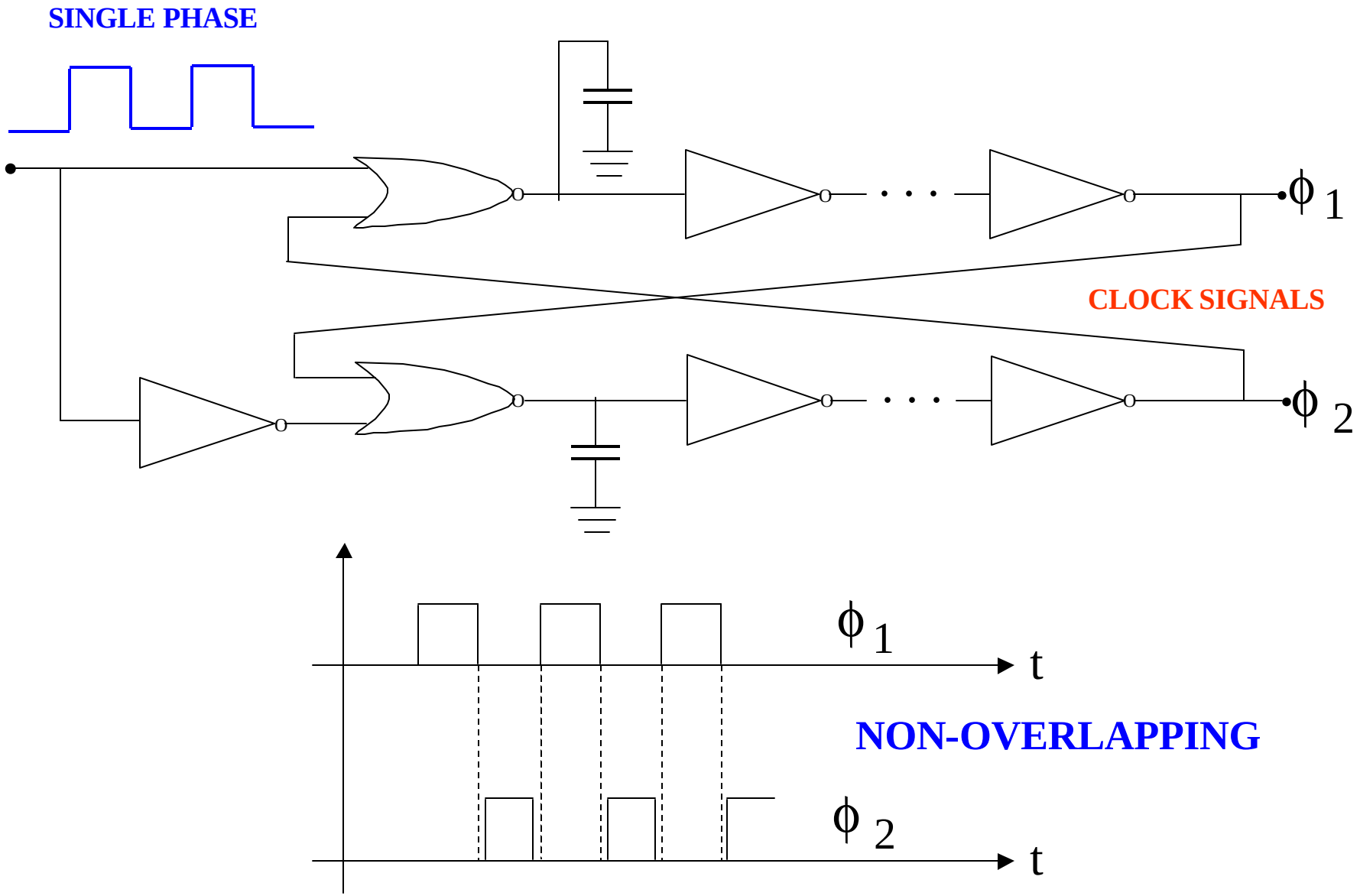
CONVENTIONAL NOTATION FOR TRANSFER FUNCTION IS:

$$H^{ij}(Z) = \frac{V_o^{j}(Z)}{V_{in}^{i}(Z)}$$

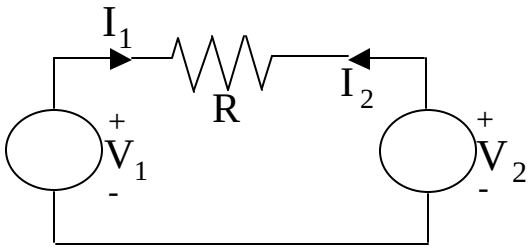
i and *j* can be either “e” or “o”. i,e.,

$$H^{eo}(Z) = \frac{V_o^{o}(Z)}{V_{in}^{e}(Z)}$$

TWO-PHASE CLOCK GENERATOR



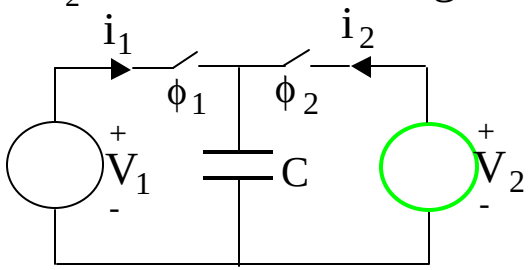
SWITCHED-CAPACITOR EQUIVALENT RESISTOR

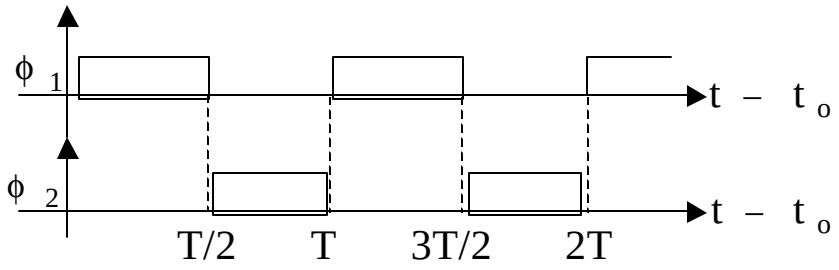


Continuous (Conventional) Resistor

$$R = \frac{V_1 - V_2}{I_1} = \frac{V_2 - V_1}{I_2} \Rightarrow I_2 = \frac{V_2 - V_1}{R}$$

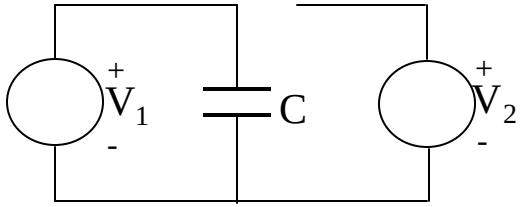
V_1 and V_2 are constant voltage sources





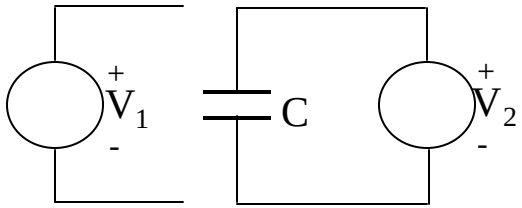
At time $t = t_o$ we apply the clocks.

At ϕ_1



$$Q(t_o + T/2) = CV_1$$

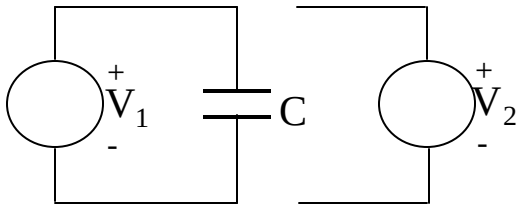
At ϕ_2



$$Q(t_o + T) = CV_2 - CV_1$$

$$Q(t_o + T) = C(V_2 - V_1)$$

For the next period, at ϕ_1



$$Q(t_o + \frac{3T}{2}) = C(V_1 - V_2)$$

$$i = \frac{dQ}{dt}$$

$$Q_1 = \int_{t_o + T}^{t_o + 3T/2} i_1(t)\,dt = \int_{t_o + T/2}^{t_o + 3T/2} i_1(t)\,dt$$

The average current $I_{1\ (aver\ )}$ becomes

$$I_{1\ (aver\ )} = \frac{Q\ (t_o + \frac{3T}{2})}{T}$$

$$I_{1\ (aver\ )} = \frac{1}{T} \int_{t_o + 3T/2}^{t_o + 3T/2} i_1(t)\, dt$$

$$I_{1\ (aver\ )} = \frac{C\ (V_1 - V_2}{T} = \frac{\Delta Q}{\Delta t}$$

or

$$\frac{T}{C} = \frac{V_1 - V_2}{I_{1\ (aver\ )}}$$

Comparing with the continuous time resistor

$$R_{eq} = \frac{T}{C} = \frac{1}{f_C C}$$

EXAMPLE. $R = 250K\Omega$, $f_C = 128KHz$

$$\frac{A_R}{A_C} \cong 32$$

$$C = \frac{1}{R_{eq} f_C} = \frac{1}{250 \times 128 \times 10^6} = 31.25pF$$

	Continuous R	"SC-R"	
AREA	5,776	178.57	mils ^{2}

ACCURACY OF TIME CONSTANTS

⊙ CONTINUOUS TIME:

$$\tau = R_1 C_2$$

$$\frac{d\tau}{\tau} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} \rightarrow \pm 40\% \rightarrow \pm 65\%$$

where $\frac{d\tau}{\tau}$ is interpreted as the accuracy of τ.

TEMPERATURE DEPENDANT!

⊙ DISCRETE TIME:

$$\tau = \frac{1}{f_C C_1} \cdot C_2 = T\left(\frac{C_2}{C_1}\right)$$

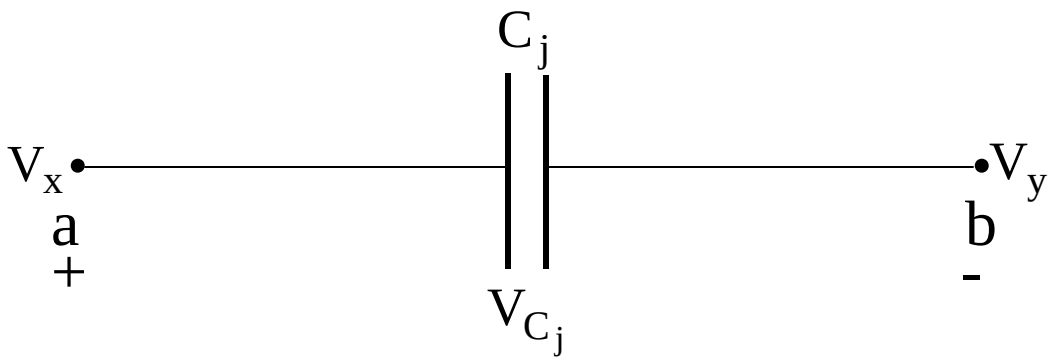
$$\frac{d\tau}{\tau} = \frac{dT}{T} + \frac{dC_2}{C_2} - \frac{dC_1}{C_1}$$

$$\frac{d\tau}{\tau} \cong \frac{dC_2}{C_2} - \frac{dC_1}{C_1} \rightarrow 0.1\%$$

KC_HL KIRCHOFF "CHARGE" LAW

$$\sum_{i=1}^{n} Q_i = 0$$

$$Q_j = C_j V_{C_j}$$



at $t = t_2$

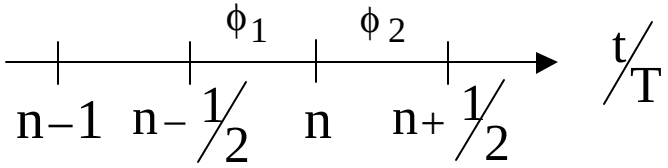
$$V_{C_j} = V_x(t_2) - V_y(t_2) - (V_x(t_1) - V_y(t_1))$$

Voltage across the capacitor V_{C_j} = voltage difference (at present time) across the capacitor minus initial condition (at past time).

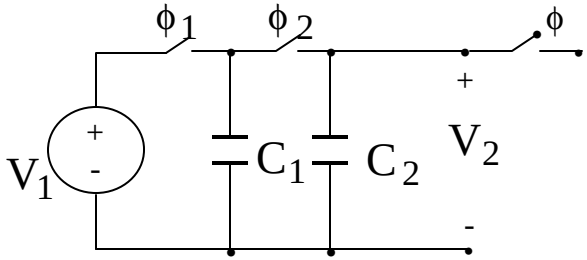
CHARGE CONSERVATION

ANALYSIS METHOD

$$q_L(n) = q_M(n-1) + \hat{q}_C(n)$$



EXAMPLE



for ϕ_2

$$C_2[V_2^e(n) - V_2^o(n-\tfrac{1}{2})] + C_1[V_2^e(n) - V_1^o(n-\tfrac{1}{2})] = 0$$

for ϕ_1

$$C_2[V_2^o(n-\tfrac{1}{2}) - V_2^e(n-1)] = 0 \Rightarrow V_2^o(n-\tfrac{1}{2}) = V_2^e(n-1)$$

THEN

$$C_1 v_2^o(n) + C_2 v_2^o(n) = C_2 v_2^o(n-1) + C_1 v_1^o(n-1)$$

$$(C_1 + C_2) V_2^o(Z) - C_2 Z^{-1} V_2^o(Z) = C_1 V_1^o(Z) Z^{-1}$$

$$H^{oo}(Z) = \frac{\frac{C_1}{C_1} Z^{-1}}{\frac{C_1 + C_2}{C_1} - \frac{C_2}{C_1} Z^{-1}} = \frac{Z^{-1}}{1 + \alpha - \alpha Z^{-1}}$$

$$H^{oo}(Z) = \frac{\frac{C_1}{C_1} Z^{-1}}{\frac{C_1 + C_2}{C_1} - \frac{C_2}{C_1} Z^{-1}} = \frac{Z^{-1}}{1 + \alpha - \alpha Z^{-1}}$$

$$H^{oo}(Z) = \frac{V_o^o(Z)}{V_{in}^o(Z)} = \frac{V_o^e(Z) Z^{-1/2}}{V_{in}^o(Z)}$$

$$V_2^e(n) = V_2^e(n + \tfrac{1}{2})$$

$$C_2[V_2^o(n + \tfrac{1}{2}) - V_2^o(n - \tfrac{1}{2})] + C_1[V_2^o(n + \tfrac{1}{2}) - V_1^o(n - \tfrac{1}{2})]$$

$$C_2[V_2^o(Z)][Z^{\frac{1}{2}} - Z^{-\frac{1}{2}}] + C_1 V_2^o(Z) Z^{\frac{1}{2}} = C_1 V_1^o(Z) Z^{-\frac{1}{2}}$$

$$C_2(1 - Z^{-1})V_2^o(Z) + C_1 V_2^o(Z) = C_1 V_1^o(Z) Z^{-\frac{1}{2}}$$

$$\frac{V_2^o(Z)}{V_1^o(Z)} = \frac{C_1 Z^{-1}}{C_2(1 - Z^{-1}) + C_1} = \frac{C_1 Z^{-1}}{C_2 + C_1 - C_2 Z^{-1}}$$

$$\frac{V_2^o(Z)}{V_1^o(Z)} = \frac{C_1}{(C_2 + C_1)Z - C_2}\Bigg| = \frac{C_1}{(C_2 + C_1) + (C_2 + C_1)ST - C_2}$$

$$Z \cong 1 + ST$$

For high-sampling rate $\omega T << 1$

$$\frac{V_2^o(Z)}{V_1^o(Z)} = \frac{C_1}{C_1 + (C_2 + C_1)5T} = \frac{1}{1 + (\frac{C_2 + C_1}{C_1})5T} = \frac{1}{1 + \cancel{5} \diagup \frac{C_1}{(C_2 + C_1)T}}$$

$$Z \cong 1 + ST$$

$$f_{3d\beta} \cong \frac{1}{2\pi} \cdot \frac{C_1}{(C_2 + C_1)T} = \frac{1}{2\pi} \cdot \frac{f_c}{1 + \frac{C_2}{C_1}}$$

Aside:

$$f_{3d\beta} \cong \frac{1}{2\pi} \cdot \frac{1}{R_1 C_2} \cong \frac{1}{2\pi} \cdot \frac{1}{\frac{TC_2}{C_1}} = \frac{1}{2\pi} \cdot \frac{f_c}{\frac{C_2}{C_1}}$$

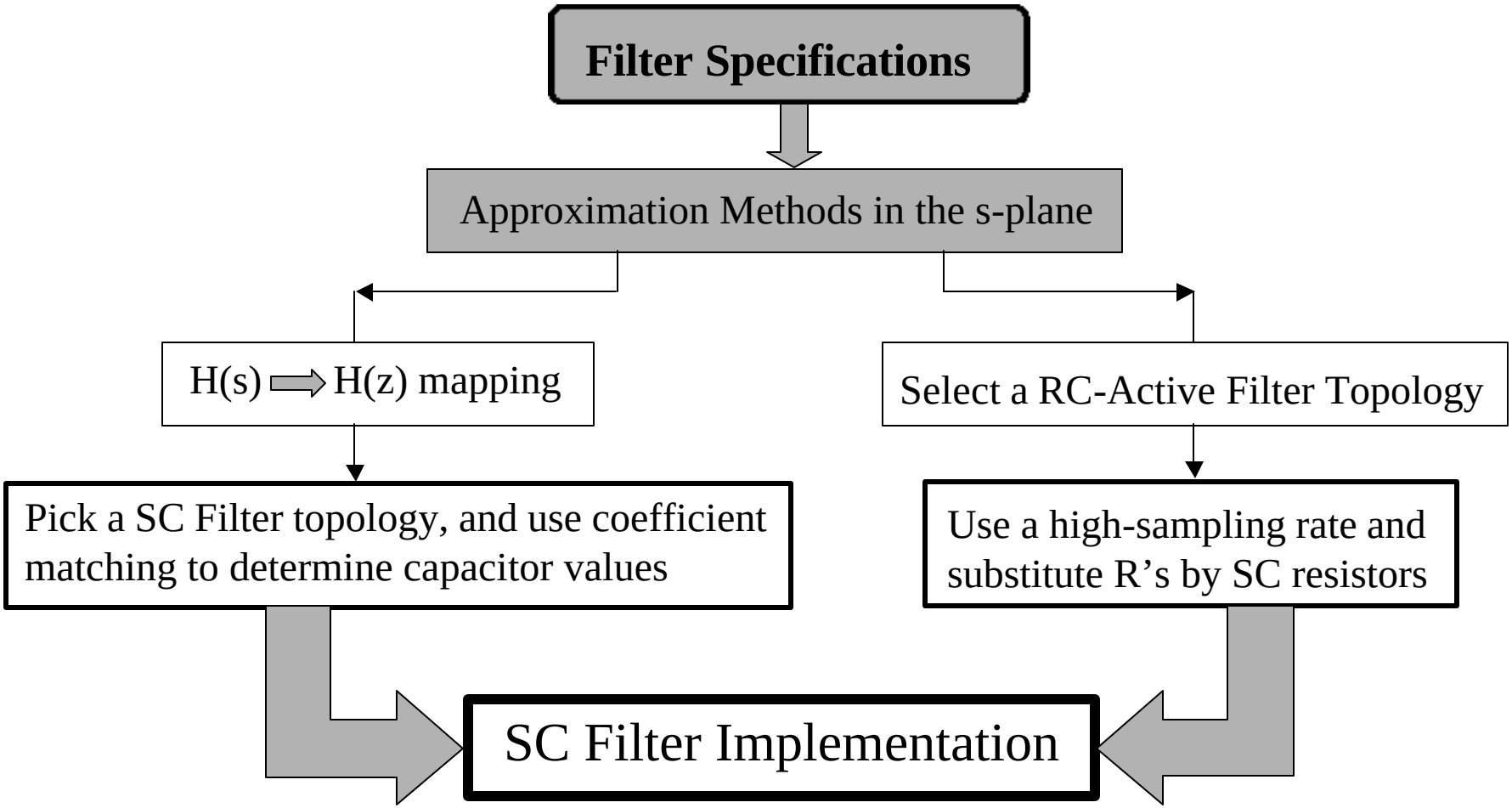
Switched-Capacitor techniques advantages

- Reduced silicon area
- Good accuracy. Time constants are implemented with capacitor ratios (~0.1%)
- Don’t require a low-impedance output stage (OTAs could be used)
- Could be implemented using digital circuit process technology
- Very useful in the audio range

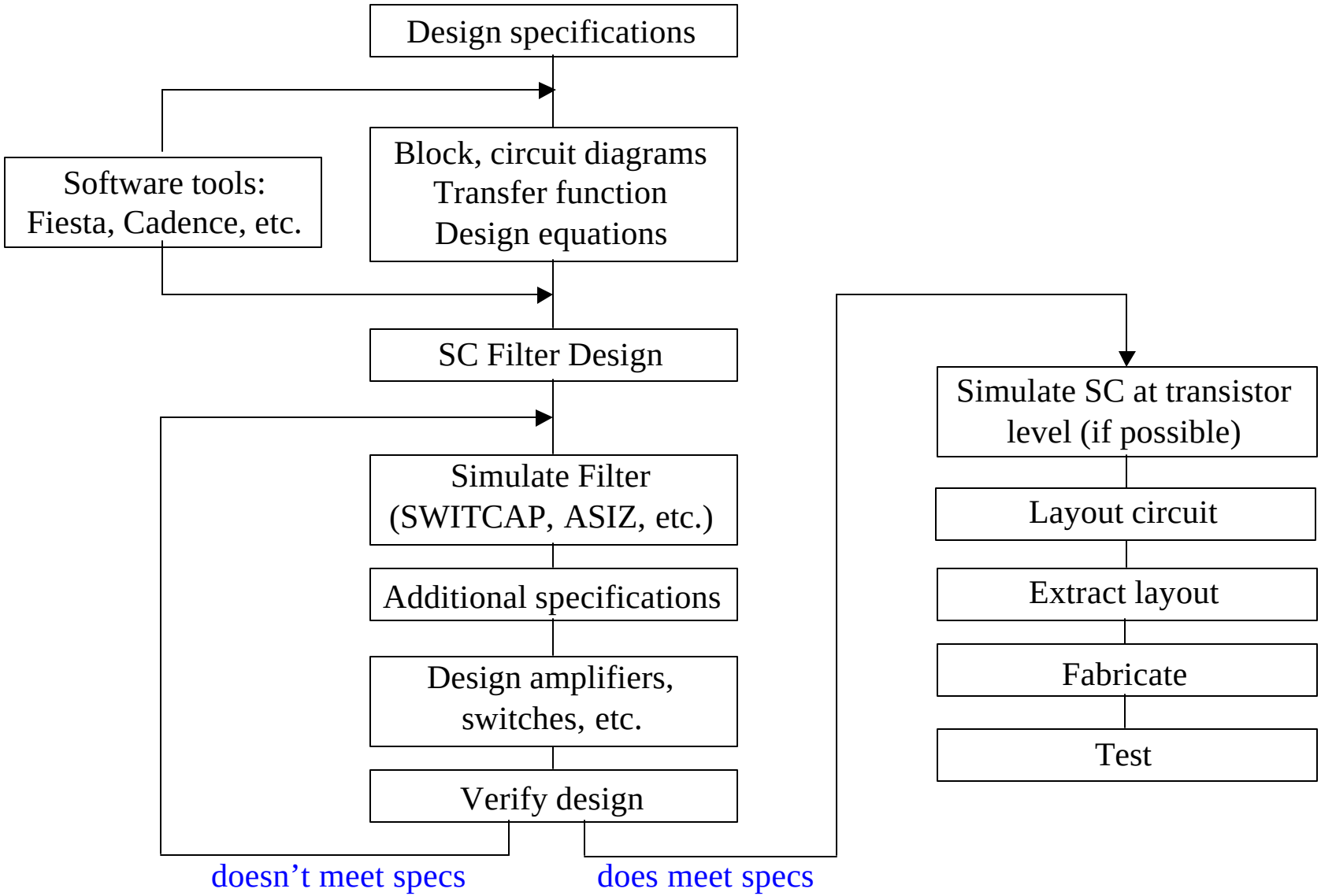
Switched-Capacitor (SC) Filters

How to design SC Filters ?

- Two basic approaches



Systematic SC Filter Design



What are the advantages and disadvantages of the two filter design procedures ?

- Mapping Techniques

  + Systematic and well documented (see FIESTA-2)

  + It can use any sampling rate, including the (minimum) Nyquist rate.

  - Difficult to implement by hand calculation

- Transforming R to SC resistors

  + It is, conceptually, easier to follow for analog designer

  + Its design is straightforward

  - Yields not an optimal design for area, imposed high sampling rate involves larger capacitor ratios.

Switched-Capacitor Filters Components

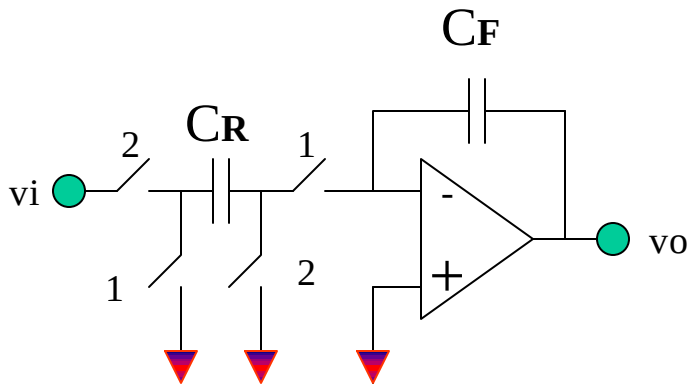
Basic Elements

Capacitors
- polysilicon
- metal1-metal2
- parasitics, clock-feedthrough

Switches
- N-MOS
- Transmission gates
- Noise and on-resistance

OTAS
- DC-gain
- settling time (GBW, phase margin)
- noise

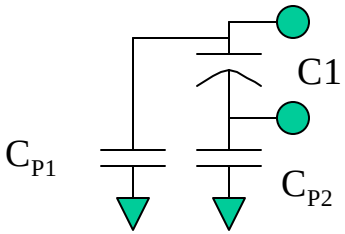
Non-overlapping clock phases

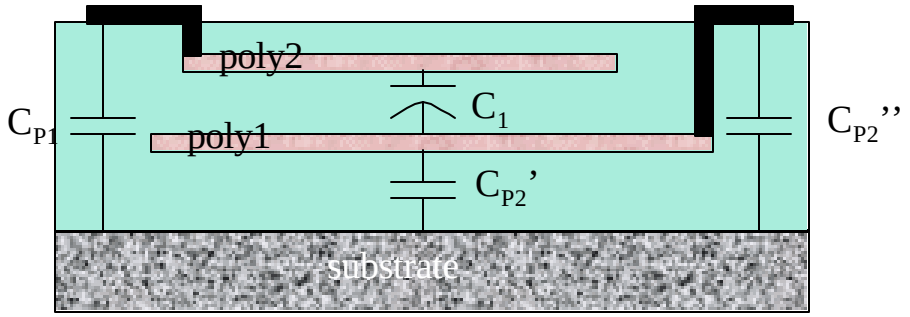


Typical switched-capacitor integrator

Switched-Capacitor Filters: CAPACITORS

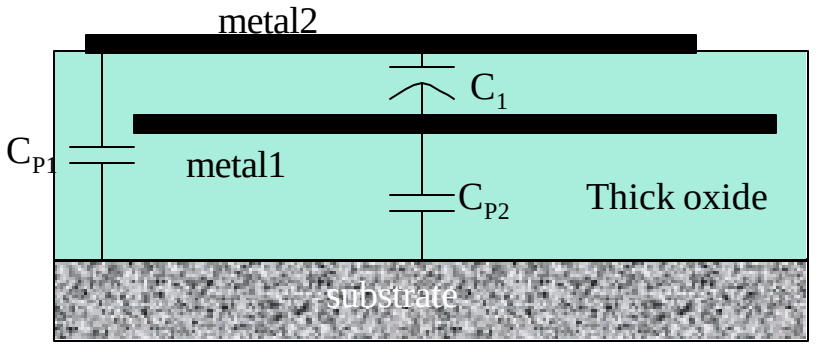
polysilicon





CP1, CP2'' are very small (1-5 % of C1)
CP2' is around 10-30 % of C1

metal1-metal2

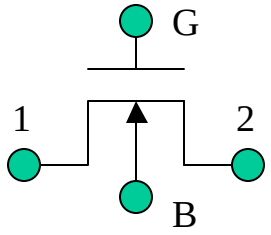


SWITCHES

MOS transistors biased in triode region, ~100-100 kw

Off resistances ~ G w

N-MOS

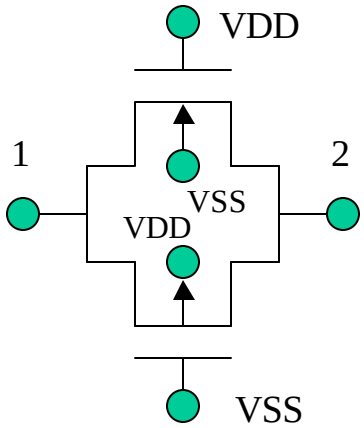


•V_1, $V_2 < V_G - V_T$ ($V_T \sim 1$ V)

• Resistance $Rs \cong \frac{L}{\mu_n C_{ox} W (V_{GS} - V_T)}$

• Small resistance for low voltages but high resistance for large voltages

• Transmission gates



• Rail to rail operation, provided that VDD and IVSSI > VT

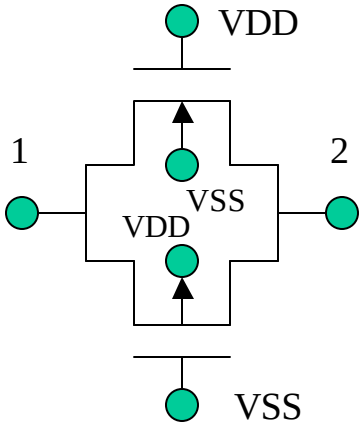
• Smaller resistance (fast response)

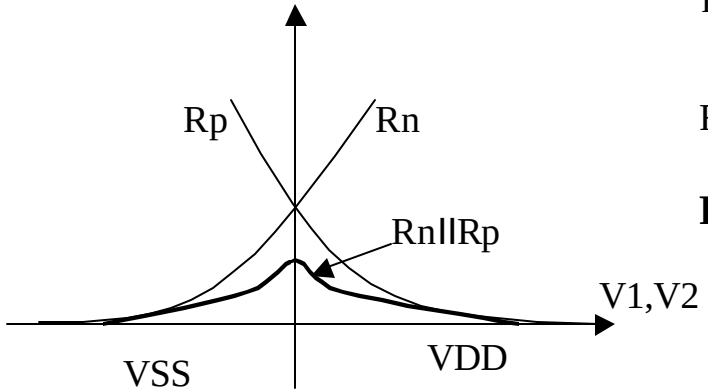
• 2 clock phases

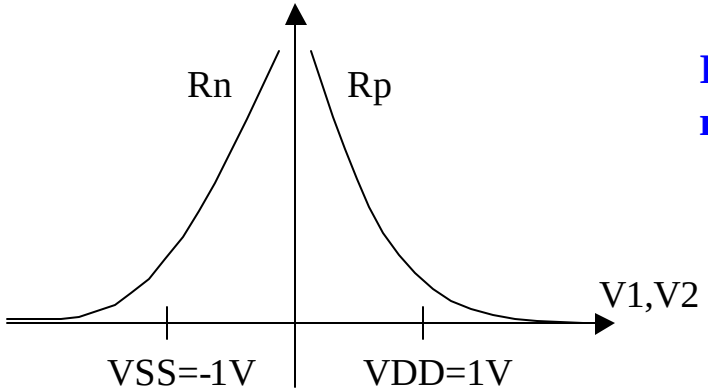
• More parasitics

Switched-Capacitor Filters: SWITCHES

Transmission gates







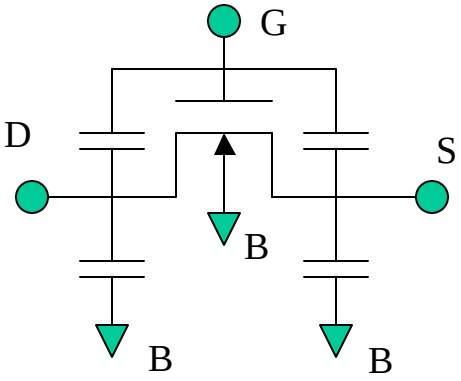
$$R_n \cong \frac{L}{\mu_n C_{ox} W(VDD - V1 - V_T)}$$

For V1, V2=0, W/L=1, $\mu_n C_{OX}=10^{-4}$

R_n=10k/(VDD-1)

If VDD, |VSS|<V_T, the resistance is extremely high!!!

Switches (continues)

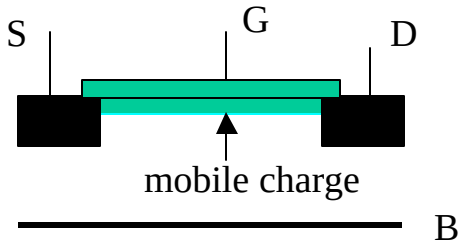


$$C_{GS,GD} = C_{OX} WL_D + \frac{1}{2} C_{OX} WL$$

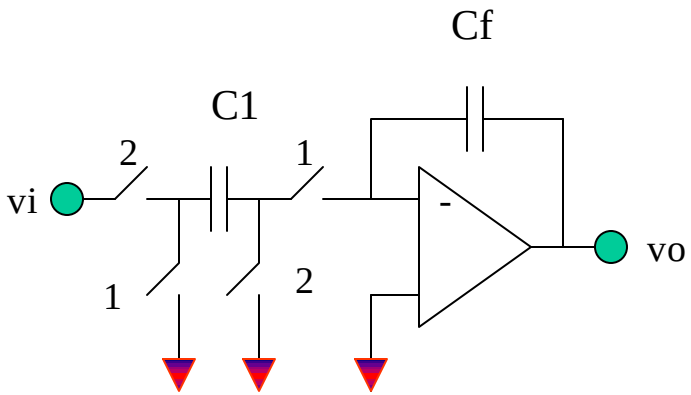
$$C_{BS,BD} = \frac{1}{2} \frac{C_{j0} WL}{\sqrt{1 + \frac{2\phi_F}{VSB}}} + C_{jBS}$$

$$\text{mobile} - \text{charge} = C_{OX} WL (V_{GS} - V_T)$$

- **CGS and CGD are Linear polysilicon capacitors, introduce offset voltage.**
- **$C_{SB,DB}$ are non-linear capacitors, introduce harmonic distortion components.**
- **Mobile charge introduces gain errors and harmonic distortion components.**



Operational Transconductance Amplifier



PRACTICAL CONSIDERATIONS:

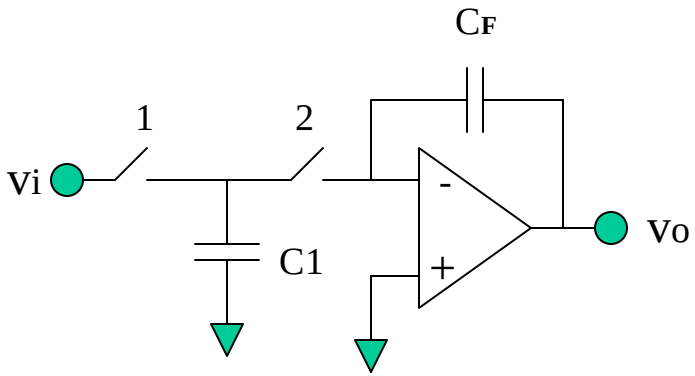
• **DC-gain**. The inverting input is not a real virtual ground. $v_{invert}=v_o/A_{dc}$

• **Settling time**. C1 must be discharged during phase 1. The main limitation is due to limited output current and phase margin.

•**Clock feedthrough.** Can be alleviated by using especial clocking schemes.

• **Noise.** In most of the practical cases the dominant noise components are due to the Switches!!!

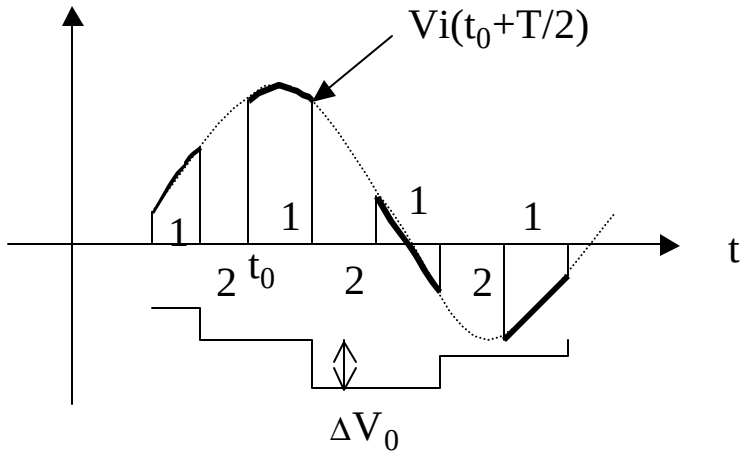
Switched-Capacitor Integrator Analysis



Basic Stray-Sensistive Integrator

Phase 1 $t_0 < t \le t_0 + T/2$

Phase 2 $t_0 + T/2 < t \le t_0 + T$



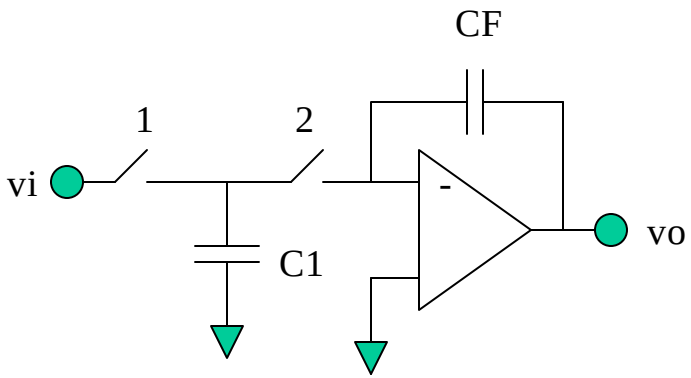
Charge conservation Principle:

Charge injected by C1 is equal to the charge absorved by CF ($DQ_{CI}=DQ_{CF}$)

$$\Delta V_0 CF = -\Delta Q_{C1}$$

$$\Delta v_0 = -\frac{C1}{CF} v_i(t_0 + NT/2)$$

Switched-Capacitor Stray-Sensitive Integrator Analysis



Basic Integrator

Phase 1 $t_0 < t \le t_0 + T/2$

$v_{C1}(t) = v_i(t)$ $\quad v_{CF}(t) = v_{CF}(t_0)$

$v_{C1}(t_0 + NT/2) = v_i(t_0 + NT/2)$ $\quad v_{CF}(t_0 + NT/2) = v_{CF}(t_0)$

Phase 2 $t_0 + T/2 < t \le t_0 + T$

Charge conservation Principle:

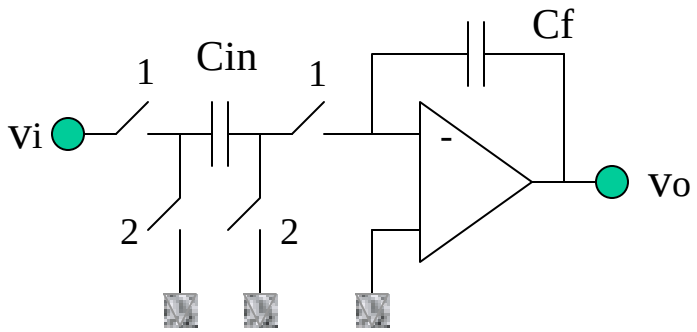
Charge injected by C1 is equal to the charge absorved by CF ($\Delta Q_{CI} = \Delta Q_{CF}$)

$$[(0-0)C_1 - (v_i(t_0 + T/2) - 0)C_1] + [(0 - v_0(t))C_f - (0 - v_0(t_0 + T/2))C_f] = 0$$

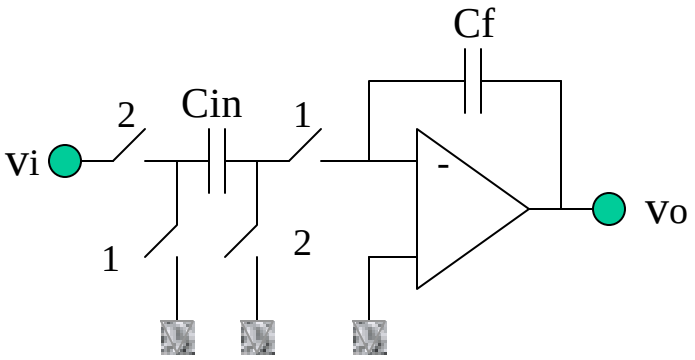
Solving for phase 2 (t=t0+T)

$$H(z) = -\frac{C_1}{C_f}\frac{z^{-1/2}}{1 - z^{-1}}$$

Switched-Capacitor Integrators : Stray-Insensitive Integrators



Backward Integrator



Forward Integrator

Charge conservation ==> Phase 1

$$(v_i(nT)-0)C_{in}+[(v_0(nT)-0)C_f-(v_0(nT-T/2)-0)C_f]=0$$

Phase 2

$$0=(v_0(nT-T/2)-0)C_f-(v_0(nT-T)-0)C_f$$

Solving for phase 1

$$v_i(nT)C_{in}-[v_0(nT)-v_0(nT-T)]C_f=0$$

$$H(z)=-\frac{C_{in}}{C_f}\frac{1}{1-z^{-1}}$$

Charge conservation ==> Phase 1

$$(0-v_i(NT-T/2))C_{in}+[(v_0(nT))C_f-(v_0(nT-T/2))C_f]=0$$

Phase 2

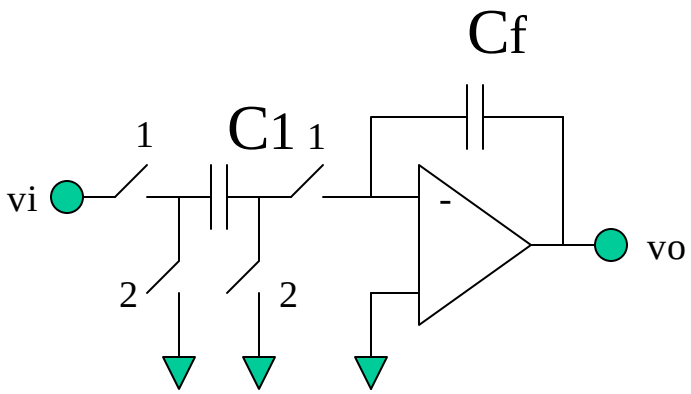
$$0=C_f v_0(nT-T/2)-C_f v_0(nT-T)$$

$$v_{cin}(NT-T/2)=v_i(NT-T/2)$$

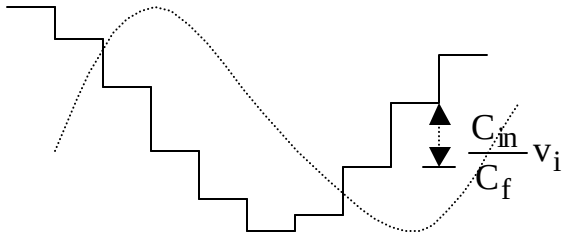
$$v_i(nT-T/2)C_{in}-[v_0(nT)-v_0(nT-T)]C_f=0$$

$$H(z)=\frac{C_{in}}{C_f}\frac{z^{-1/2}}{1-z^{-1}}$$

Switched-Capacitor Backward Integrator



Backward Integrator



phase 2

C_{in} is discharged (v_{ci}=0)
and v_{out} is constant

phase1

C_{in} is charged (v_{ci}=v_i)

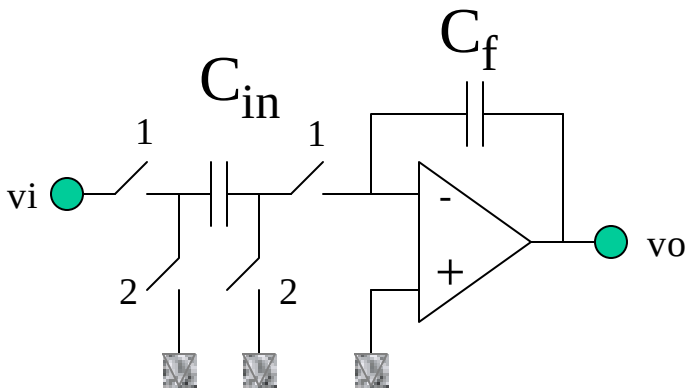
$$\Delta Q_{Cin} = C_{in} V_i \qquad \Delta Q_{Cf} = C_f (V_o(nT) - V_o(nT - T/2))$$

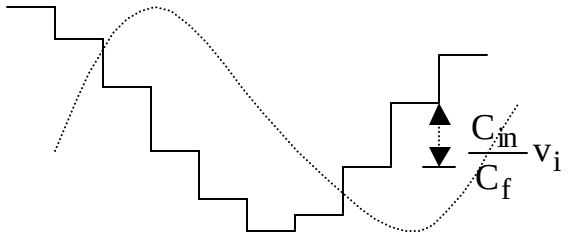
$$(v_i(nT) - 0)C_{in} + [(v_0(nT) - 0)C_f - (v_0(nT - T/2) - 0)C_f] = 0$$

or

$$v_0(nT) = v_0(nT - T) - \frac{C_{in}}{C_f} v_i(nT)$$

Switched-Capacitor Backward Integrator





Backward Integrator

phase 1

$$v_0(nT) = v_0(nT - T) - \frac{C_{in}}{C_f} v_i(nT)$$

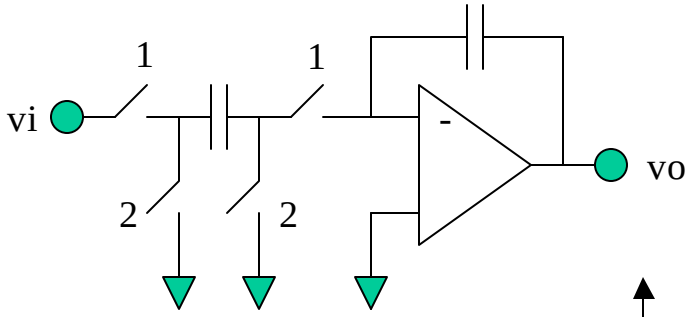
$$H^{oo}(Z) = \frac{v_0{}^o(z)}{v_i{}^o(z)} = -\frac{C_{in}}{C_f} \frac{1}{1 - Z^{-1}}$$

phase2

$$v_0(nT + T/2) = v_0(nT)$$

$$H^{eo}(Z) = \frac{v_0{}^e(z)}{v_i{}^o(z)} = \frac{Z^{-1/2} v_0{}^o(z)}{v_i{}^o(z)} = -\frac{C_{in}}{C_f} \frac{Z^{-1/2}}{1 - Z^{-1}}$$

Switched-Capacitor Integrators: Fundamental limitations

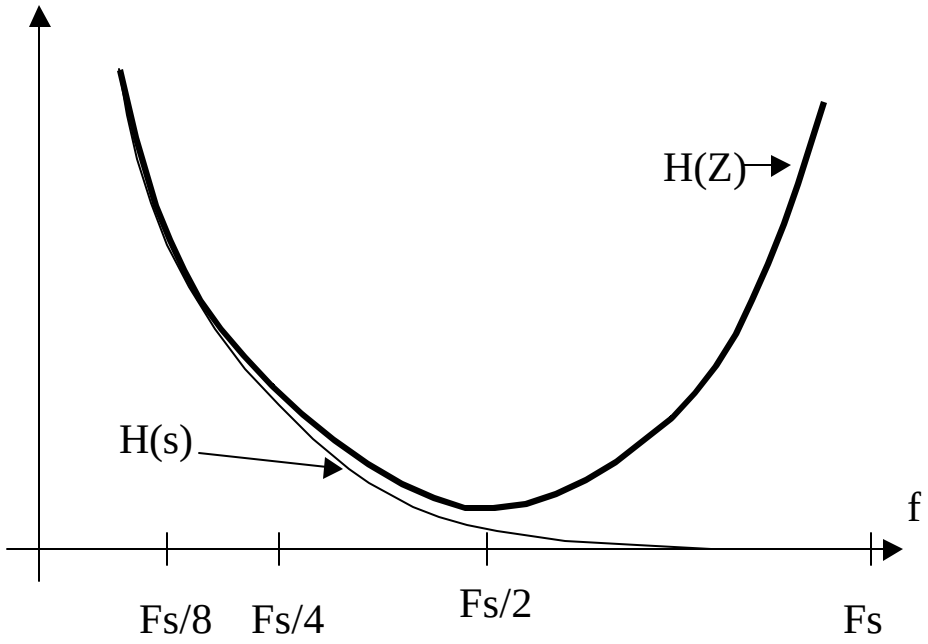


$$H^{oo}(Z) = -\frac{C_{in}}{C_f}\frac{1}{1-Z^{-1}}$$

$$Z = e^{j\omega T}$$

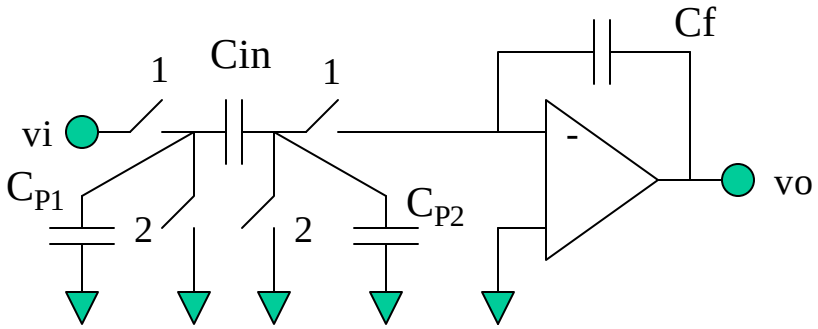
H(z=1)=∝ dc gain

H(z=-1)=-Cin/Cf Minimum gain



| H(Z) behaves as an integrator for f<fs/4

Backward (series) integrator: Why is stray insensitive???



phase2

C_{in}, C_{P1} and C_{P2} are discharged (initial conditons=0)

phase 1

C_{in} and C_{P1} are connected to Vi
C_{P2} is connected to the virtual ground (initial conditons=0)

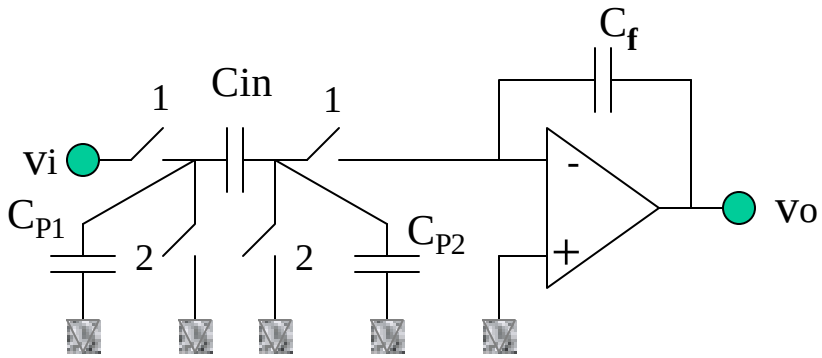
NOTE THAT

- **CP1 IS CHARGED BY vi**
- **CP2 IS CONNECTED TO GROUND OR VIRTUAL GROUND** (provided that the gain of the OPAM is large enough)

- **BOTH CP1 AND CP2 DO NOT INJECT ANY CHARGE TO CF.**

$$H^{oo}(Z) = \frac{v_0{}^{o}(z)}{v_i{}^{o}(z)} = -\frac{C_{in}}{C_f}\frac{1}{1-Z^{-1}}$$

Why SC-Circuits are important??



•**Little sensitive to parasitics** (due to the use of local feedback)

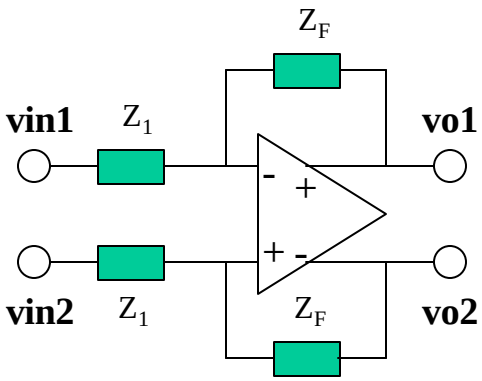
•**High precision (0.2-1 %)** (function of capacitor ratios and clock frequency)

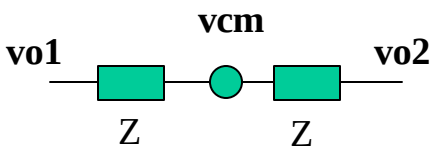
$$H^{oo}(Z) = -\left\lceil \frac{C_{in}}{C_f} \right\rceil \frac{1}{1 - Z^{-1}}$$

•**Reduced Silicon-Area** (double poly or metal-metal capacitors can be easily implemented in CMOS).

•**OPAMPS (VCVS) ARE NOT REQUIRED; OTAS ARE FASTER** (Resistors are simulated by switches and capacitors).

Fully-Differential Filters: CMFB Principle





$$v_{cm} = \frac{v_{01} + v_{02}}{2}$$

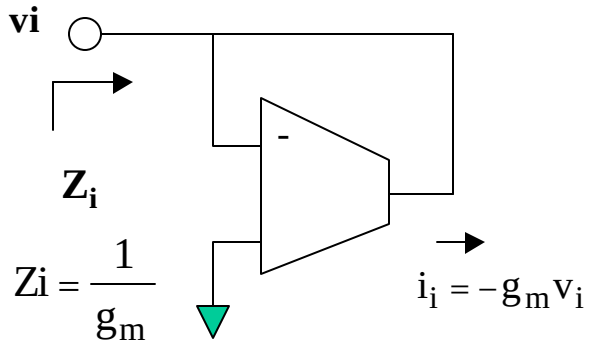
- A common-mode feedback loop must be used.

- BASIC IDEA: A circuit with very small impedance for the common-mode signas but be transparent for the differential signals.

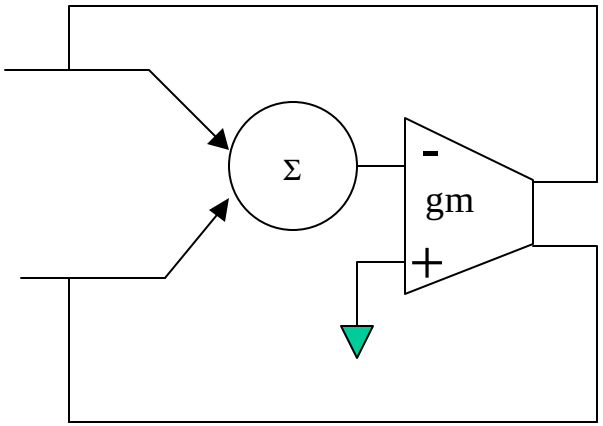
- Differential GBW similar to the GBW of the CMFB

- Minimum power consumption

Fully-Differential Filters: CMFB Principles



• A voltage controlled current source in a unity gain configuration represents a grounded impedance.



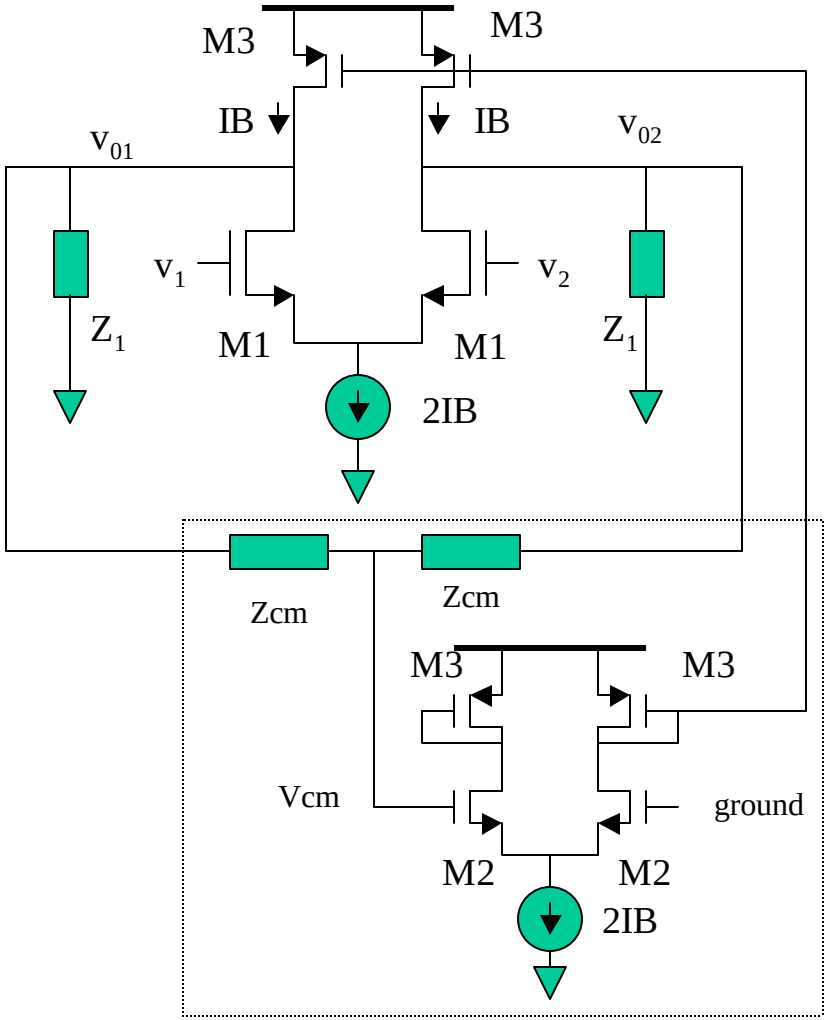
BASIC PRINCIPLE:

• The loop works for the common-mode signals.

• Ideally, the differential signals are not sensed

| common-mode impedance=1/gm

Fully-Differential Filters: CMFB Principles



CMFB

CMFB Characteristics:

| Transconductance gain=$g_{m2}/2$

| dominant pole at the output

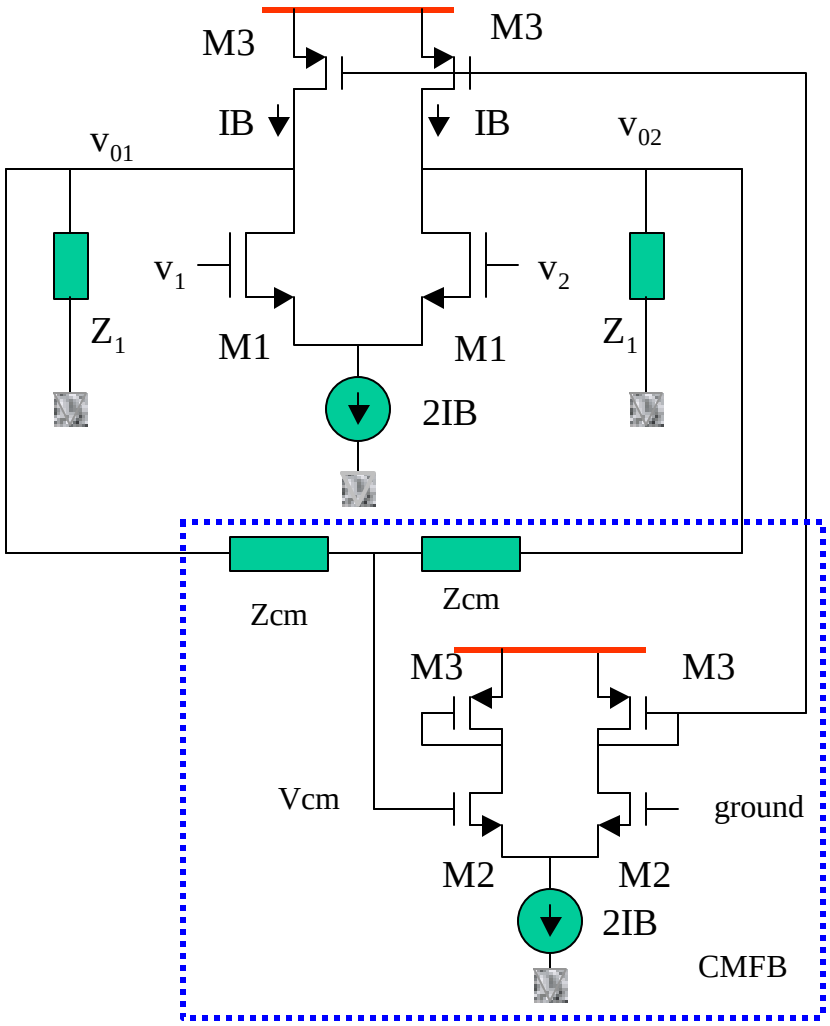
| At least 2 additional poles in the loop

| Zcm reduces the OTA dc gain, affecting the differential gain

| NOTE THAT Vcm IS FORCED TO THE GROUND LEVEL.

| DC OFFSET IS AROUND Ioff/gm2

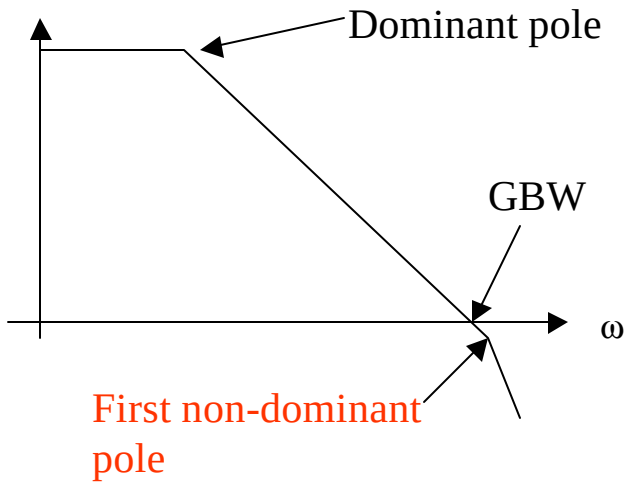
Fully-Differential Filters: CMFB Principles



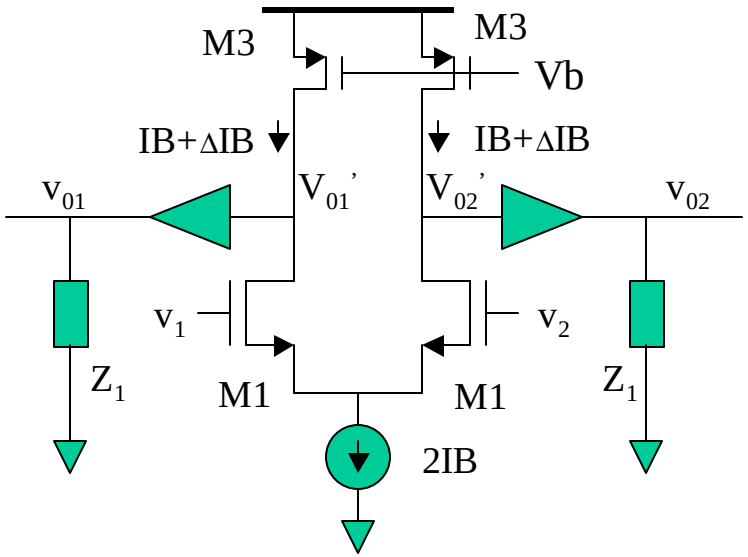
Common-mode stability:

- 1 pole at vcm (1/RC)
- 1 pole at gate of M3 (g_{m3}/C_{P3})
- 1 pole at the output (g_{01}/C_1)

| dc gain = $g_{m2}R_{01}$



Fully-Differential Filters: OPAMP

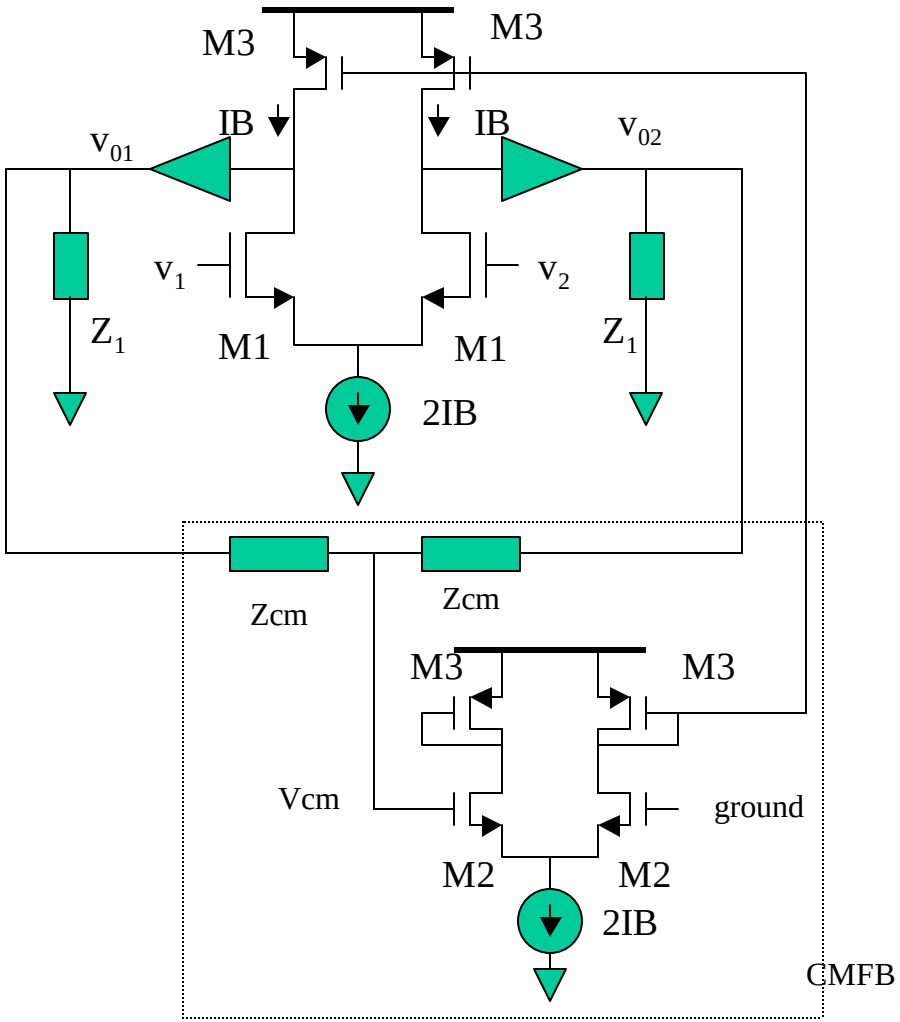


If ΔIB is positive transistors M3 eventually will be biased in triode region (small resistance)

- dc gainis drastically reduced
- THD increases
- The common-mode output impedance is the parallel of the equivalent output resistance (M1 and M3) and the parasitic capacitors. For large dc gain, the output impedance at nodes v01' and v02' are further increased.

- ΔIB produces a dc offset of $R_{out}\Delta IB$.

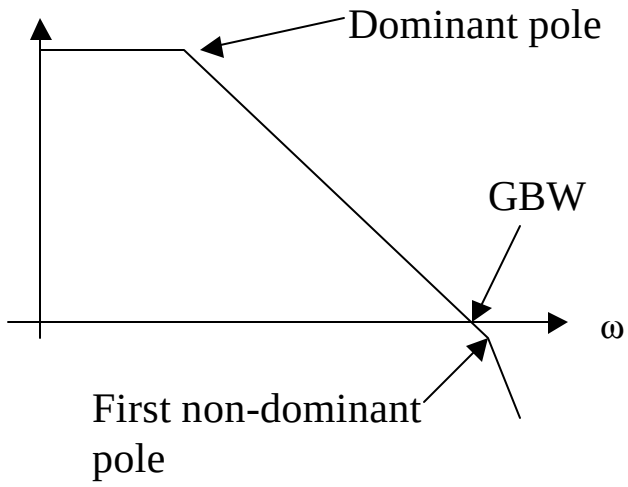
Fully-Differential Filters: OP AMP



The stability conditions are exactly the same for OTA's and OPAMP's:

- 1 pole at vcm (1/RC)

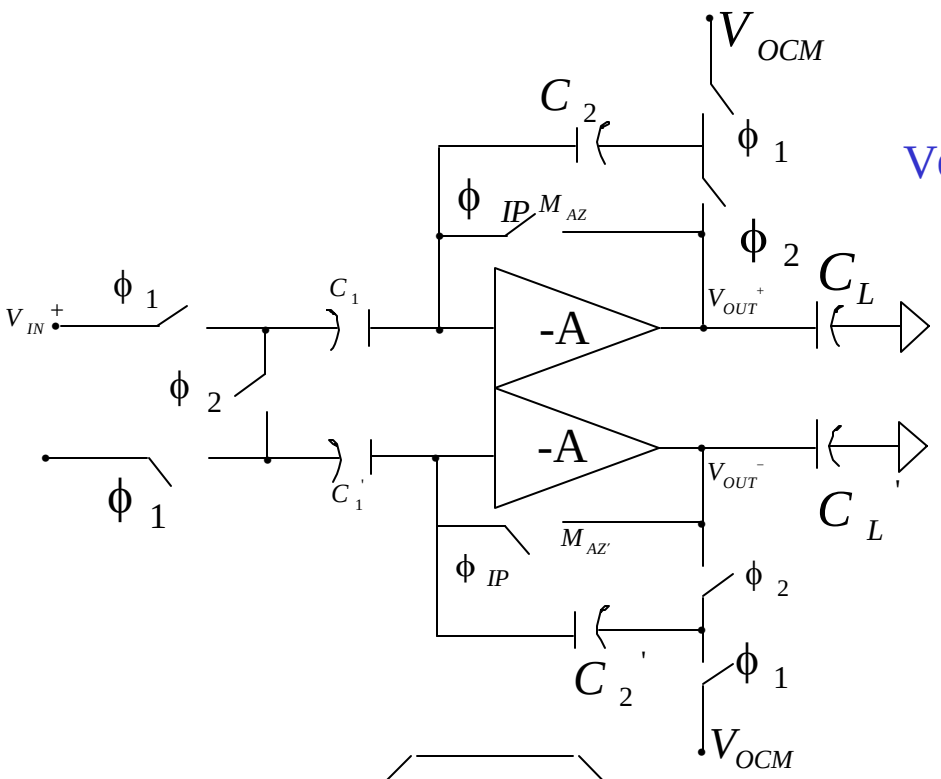
- 1 pole at gate of M3 (g_{m3}/C_{P3})
- 1 pole at the output (g_{01}/C_1)
- **In OPAMP's you can use resistors as common-mode detector due to the buffers**
- dc gain = $g_{m2}R_{01}$



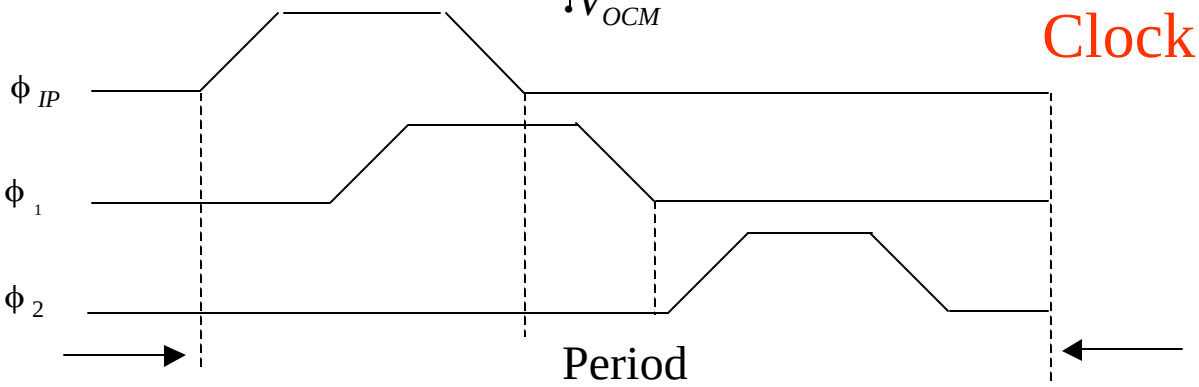
Pseudo-Differential SC Amplifier

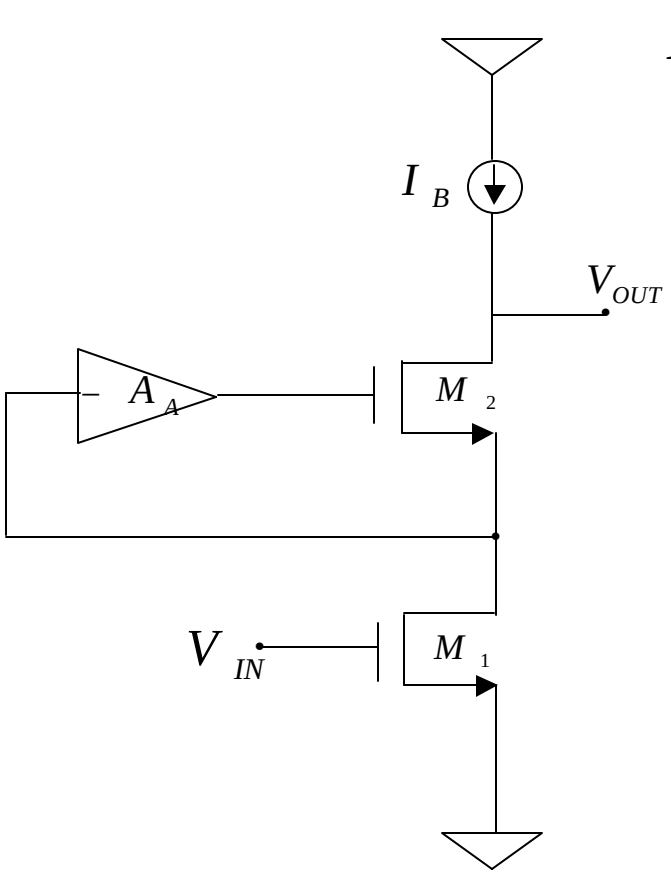
$V_{OUT}=(C_1/C_2)V_{IN}$

$V_{OUT}/V_{IN}=(C_1/C_2)/(1 + (C_1+C_2)/AC_2)$



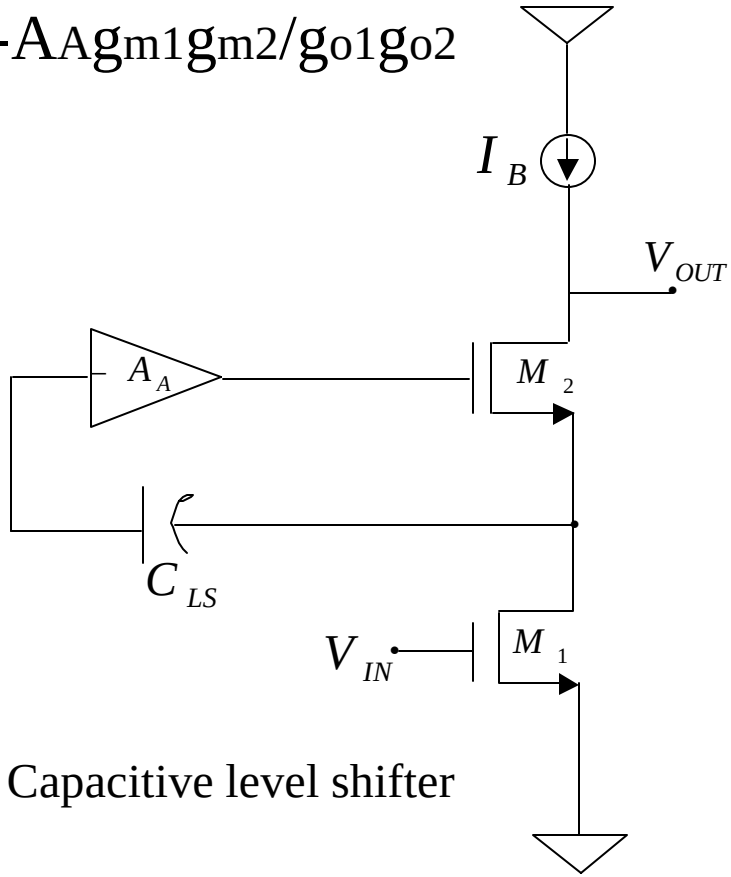
Clock Signals





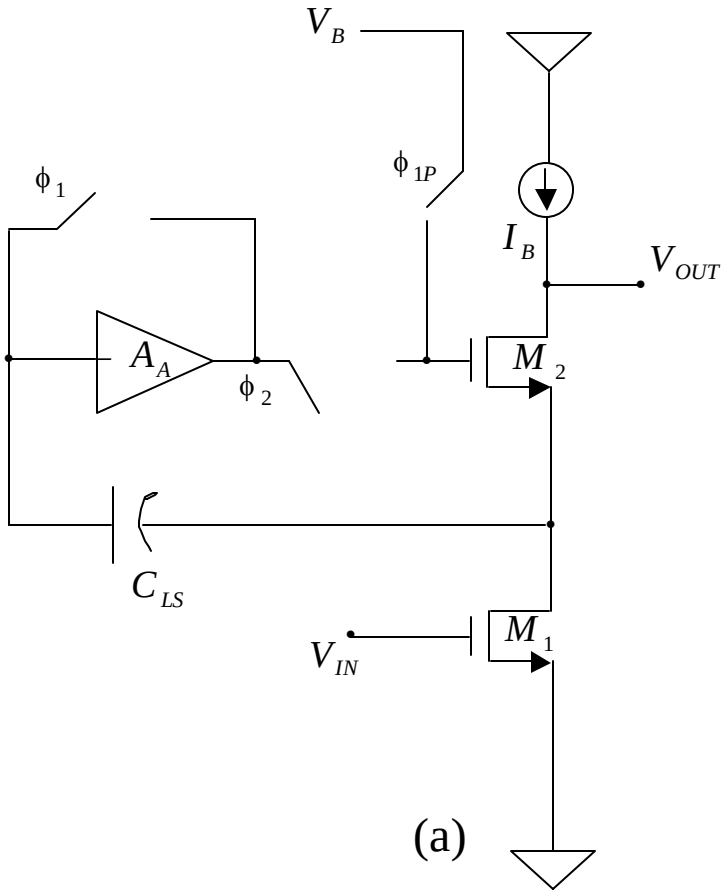
(a) Cascode transconductor with gain enhancement

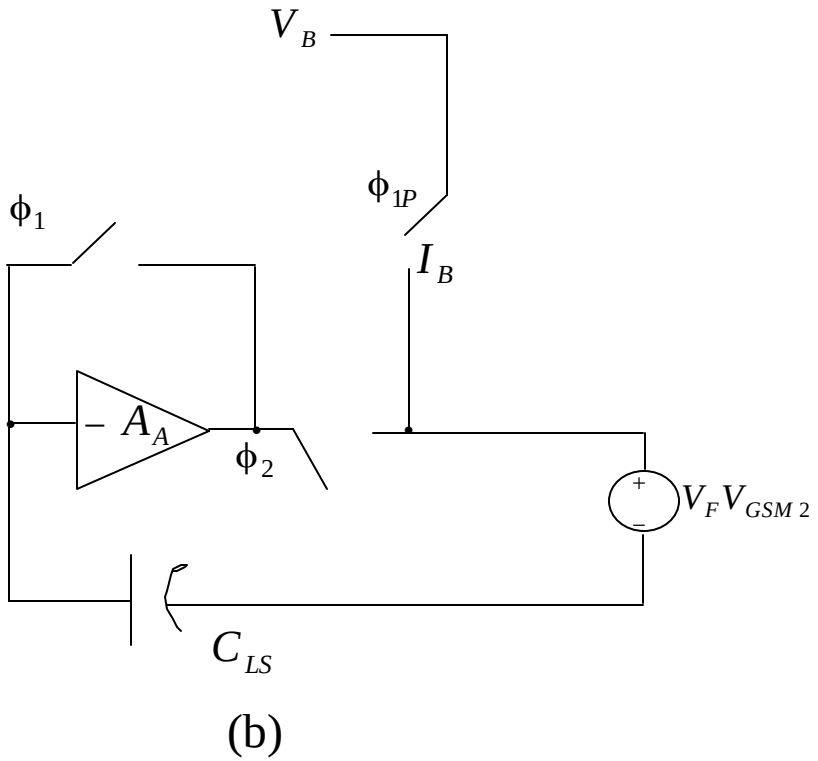
$A = -A_A g_{m1} g_{m2} / g_{o1} g_{o2}$



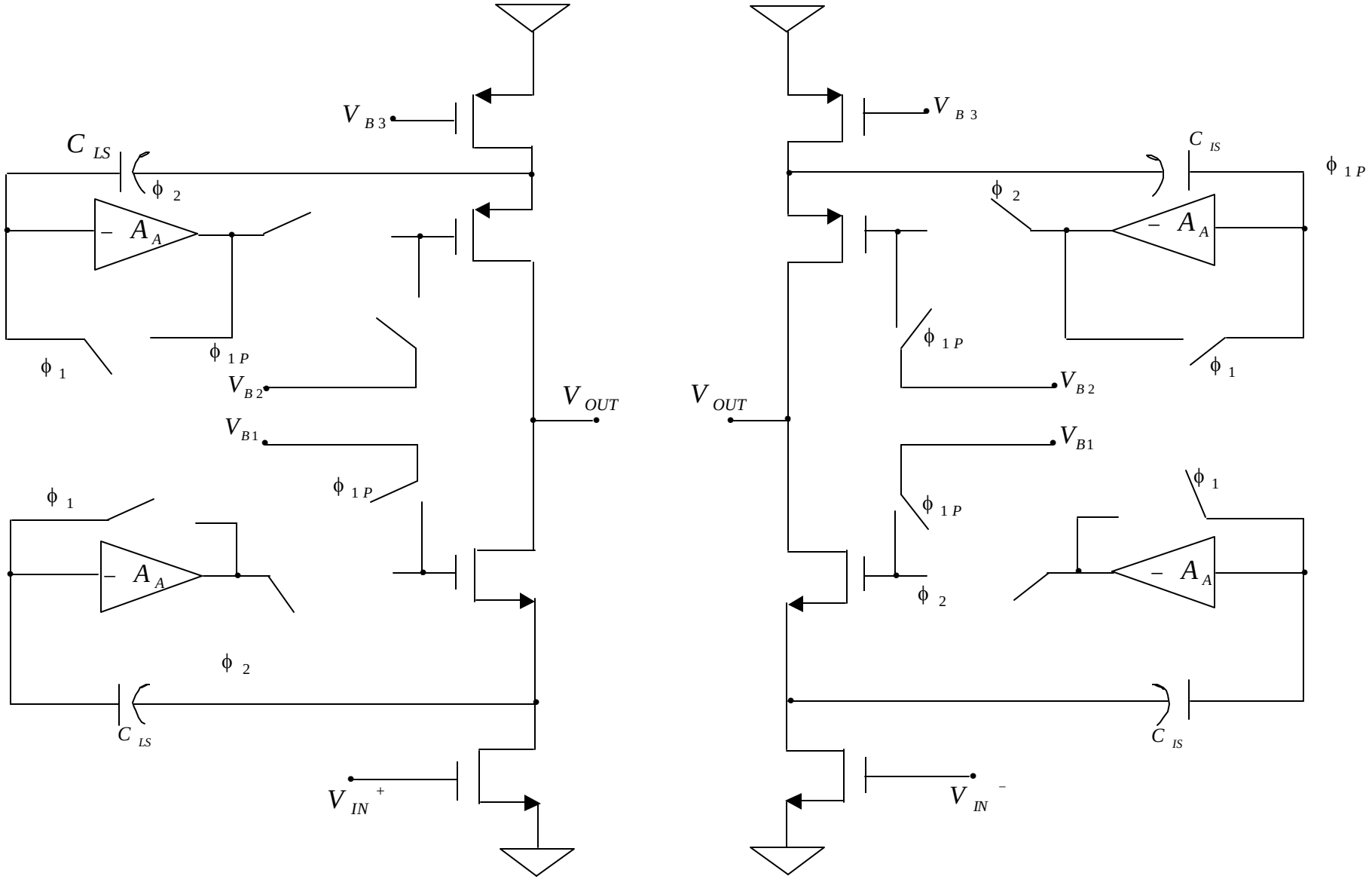
(b) Capacitive level shifter

Cascode transconductor with gain-enhancement

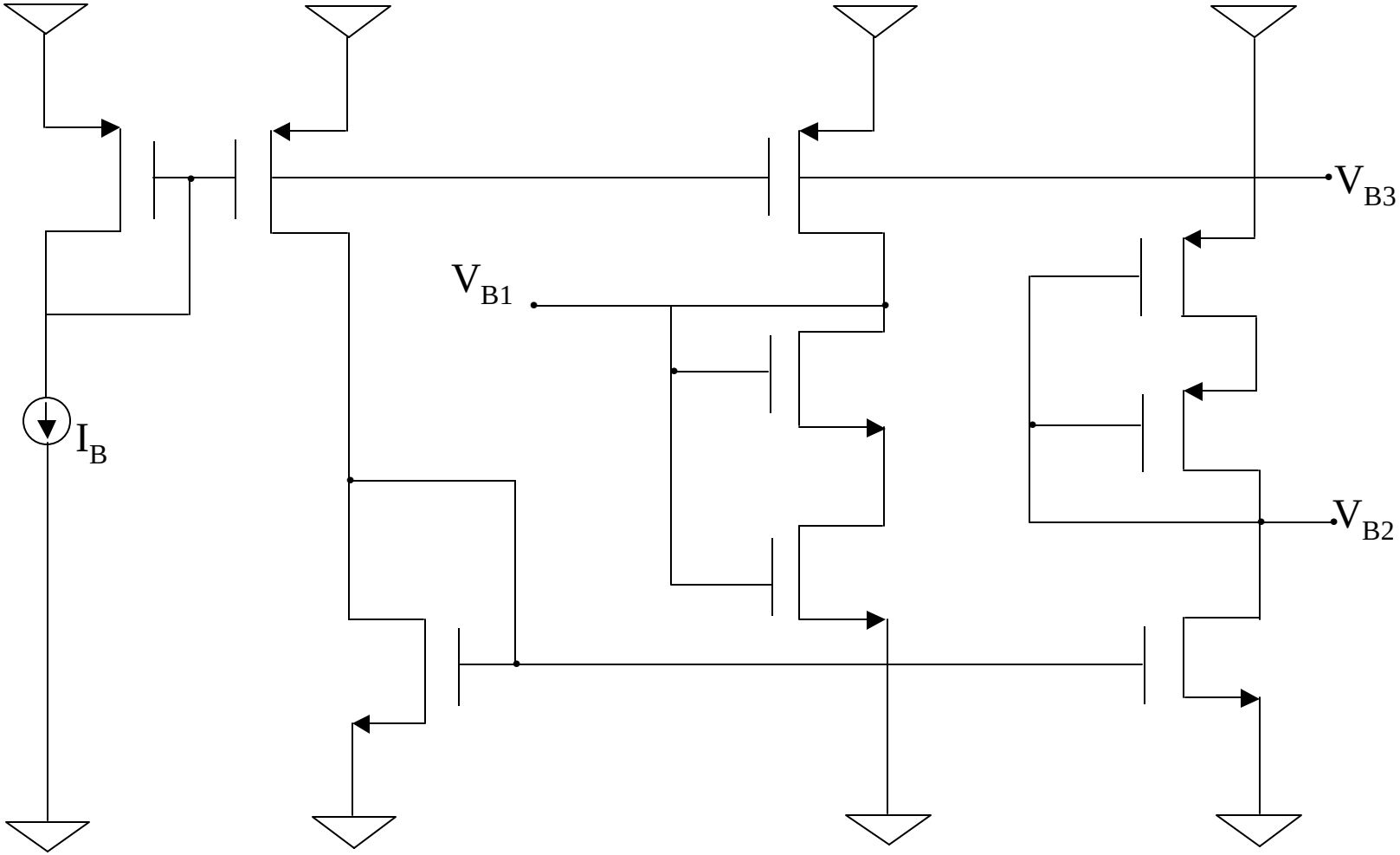




Proposed capacitive level-shifting scheme


V_{B3}
C_{LS}
ϕ_2
$-A_A$
ϕ_1
ϕ_{1P}
V_{B2}
V_{OUT}
V_{B1}
ϕ_{1P}
ϕ_1
$-A_A$
ϕ_2
C_{LS}
V_{IN}^+
V_{B3}
C_{IS}
ϕ_{1P}
ϕ_2
$-A_A$
ϕ_{1P}
V_{OUT}
V_{B2}
V_{B1}
ϕ_1
ϕ_{1P}
$-A_A$
ϕ_2
C_{IS}
V_{IN}^-

(a)



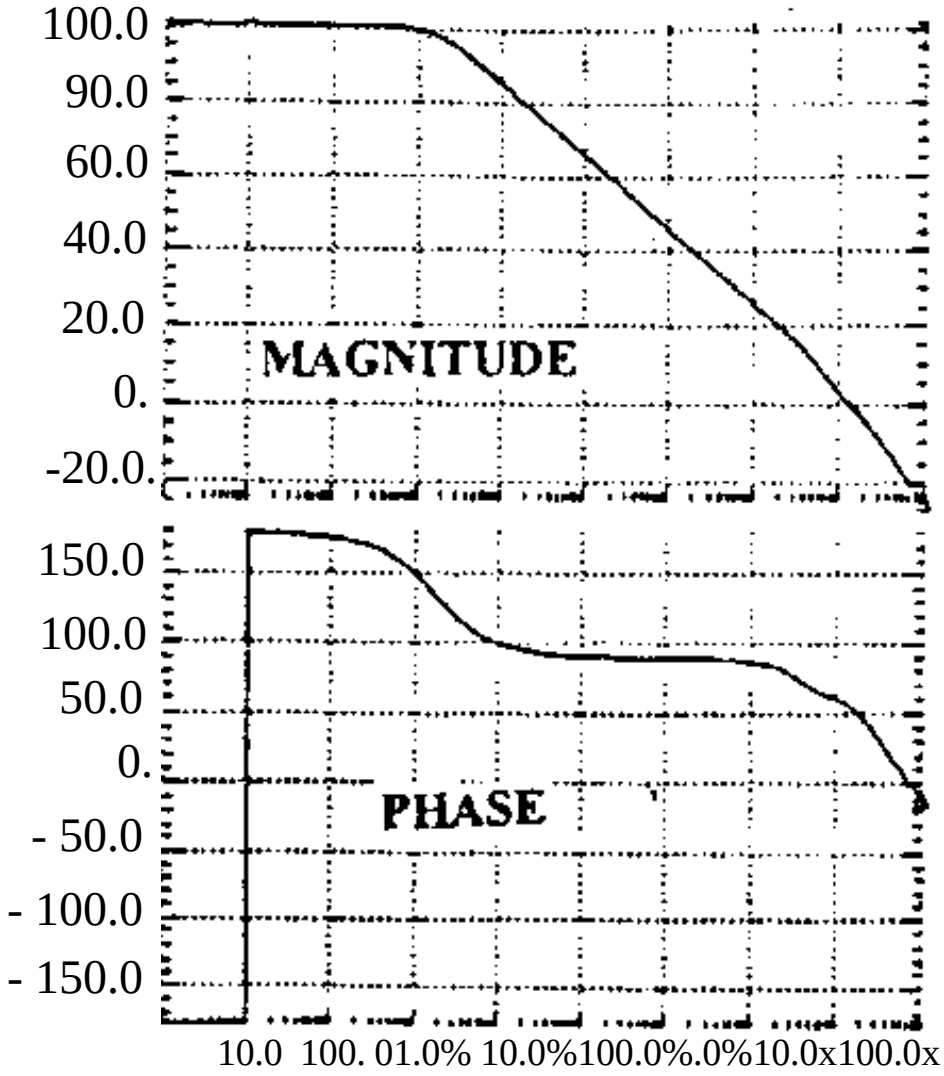
(b)

Fig. 4 (a) Pseudo-Differential core amplifier and (b) the biasing circuit

TABLE I

SUMMARY OF SIMULATED PERFORMANCE

Power Supply	1.8V
Supply Current	1.25mA
Open-Loop Gain	>100dB
U.G. Frequency	135MHz
Phase Margin	56^{o}
Input Noise	$22nV(Hz)^{1/2}$
Closed-Loop Gain	2
Gain Error	<.05%
Max. Sampling Rate	5MS/sec.
Differential Swing	1.6V


100.0
90.0
60.0
40.0
20.0
0.
-20.0.
MAGNITUDE
150.0
100.0
50.0
0.
- 50.0
- 100.0
- 150.0
PHASE
10.0 100. 01.0% 10.0%100.0%.0%10.0x100.0x

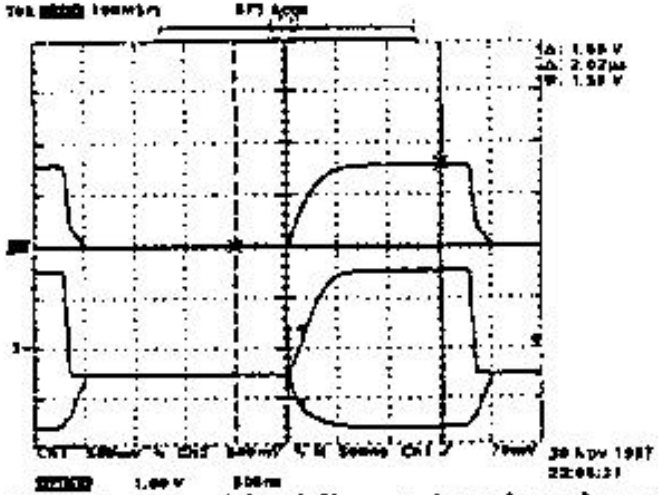


Fig.7. Settling behavior of the differential and single-ended outputs (V_{DD}=1.8V, V_{IN}=800mV).

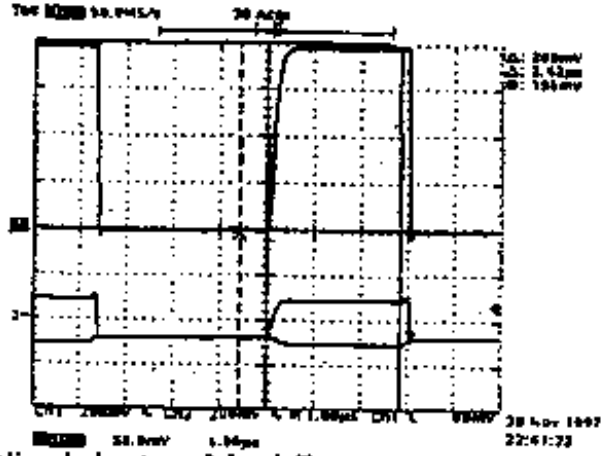


Fig.8. Settling behavior of the differential and single-ended outputs (V_{DD}=1.5V, V_{IN}=100mV).

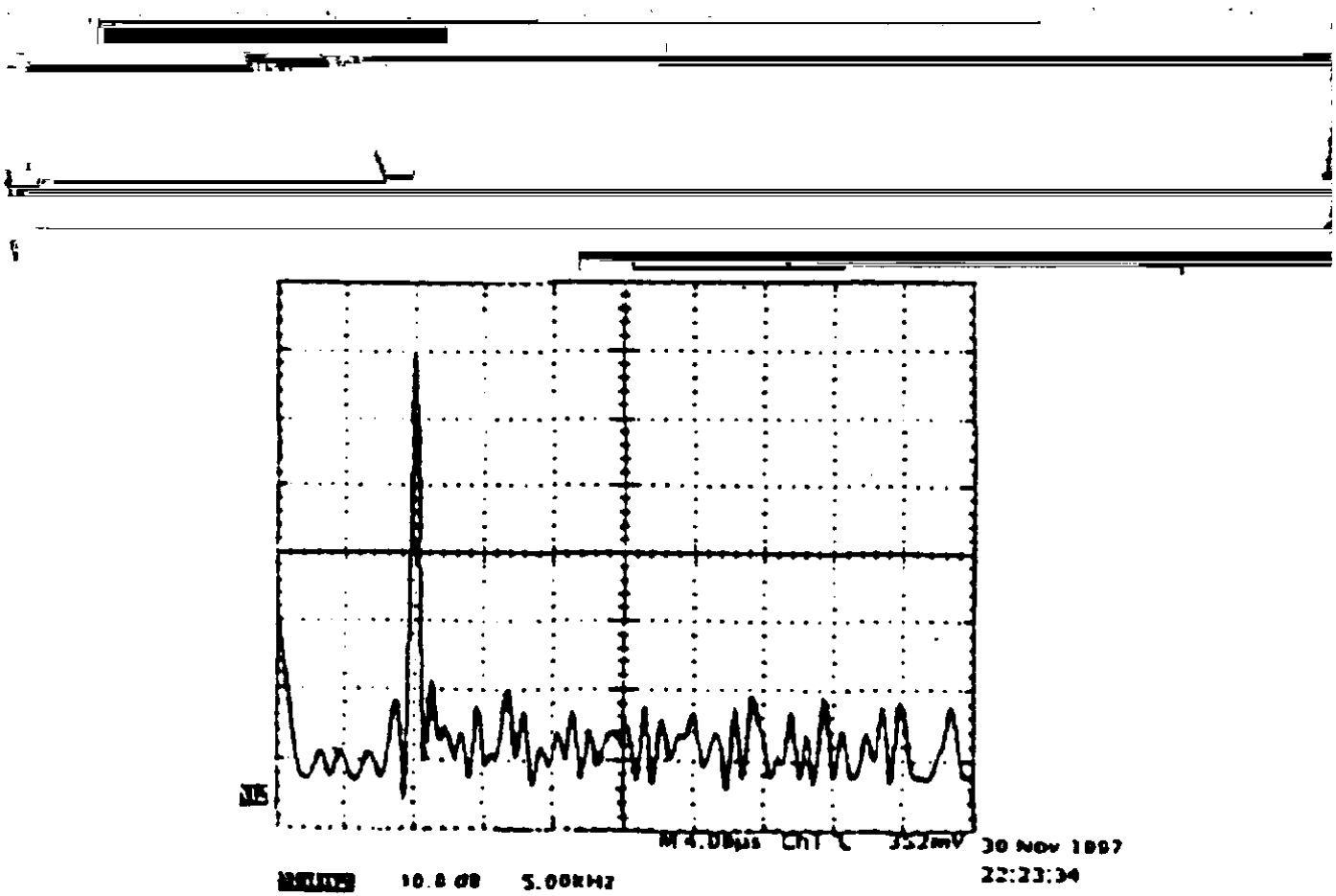


Fig.9. The frequency spectrum of the differential output.

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[3] Low-Voltage Low Power Integrated Circuits, E. Sánchez-Sinencio and A. Andreou, IEEE Press, 1999

[4] Switched Capacitor Circuits, P. E. Allen and E. Sánchez-Sinencio, Van Nostrand and Reinhold Co. 1984