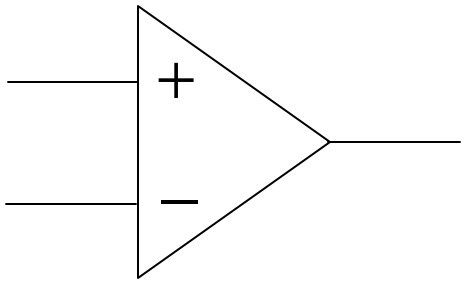
PRACTICAL CONSIDERATIONS FOR OP AMPS

Key op amp specifications:

- Gain
- Speed (BW)
- Supply voltages
- Output swing
- Noise
- Power



NON-IDEAL EFFECTS OF OP AMPS

A. FINITE DC GAIN

For a two integrator biquadratic filter:

$$\omega_{o_A} = \frac{A_o}{1+A_o}\omega_o \qquad Q = \frac{1}{\frac{1}{Q}+\frac{2}{A_o}} \cong \left(1-\frac{2Q}{A_o}\right)Q$$

Therefore:

- ω_o deviations are negligible

- Q deviations can be significant

B. FINITE BANDWIDTH

- Bandwidth is very critical for high frequency applications

How to determine the GB of an Op Amp?

- The required GB is a function of the clock frequency and the feedback topology around the Op Amp.

- A rule of thumb to select GB requires to satisfy the following inequality:

$$a\,GB\,T > 5$$

where T is the period of the clock frequency, a is the capacitor ratio between the sum of all the feedback capacitors divided by the sum of all the capacitors connected to the input terminal of the Op Amp

MULTI-STAGE OP AMP DESIGN

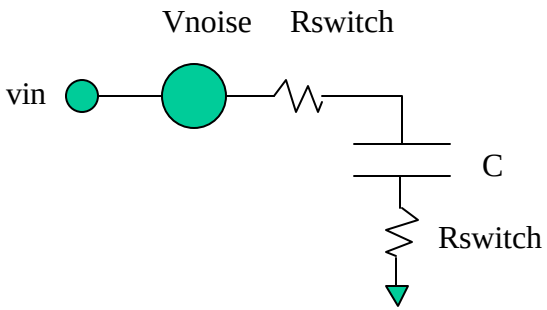
A. SINGLE-ENDED CONFIGURATION

- High gain
- CMRR = 0
- Nested compensation trades BW for stability

B. FULLY DIFFERENTIAL CONFIGURATION

- High gain
- Good CMRR
- Rail-to-rail output swing
- Higher bandwidth (less compensation)
- Requires and additional CMFB and dynamic reset

Noise due to the switches



| The switch noise density can be expressed as

$$v_{sw,noise}^{\ 2} = 4kTRswitch$$

| because two switches are present

$$v_{sw,total}^{\ 2} = 8kTRswitch \int_{BW} df = \frac{4kTRswitch}{\pi RswitchC}$$

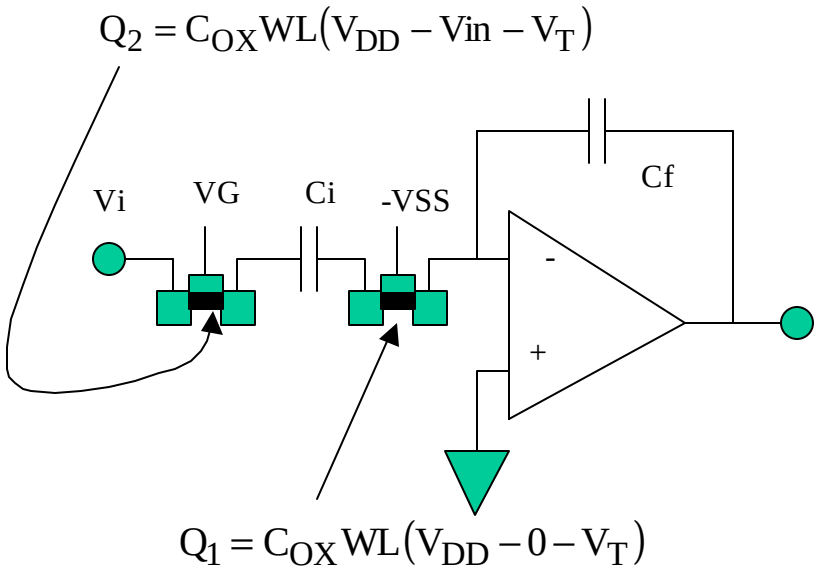
or

$$v_{sw,total} = \sqrt{\frac{4kT}{\pi C}}$$

$4kT = 16 \times 10^{-21} V^2 C$

For C=1 pF the noise level is around 70 mV

C=10 pF ==> noise level is around 20 mV



Clock Feedthrough

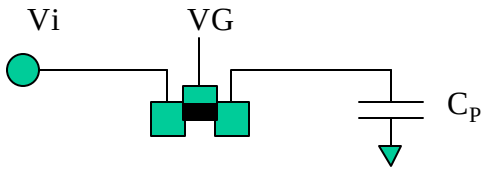
| The charge in the channel is

$$Q_{mobile} = C_{OX}WL(V_{GS} - V_T)$$

| When the switch is opened the mobile charge, ideally, should be injected to v_{in}, otherwise an error proportional to Q-channel is induced.

Basic principle

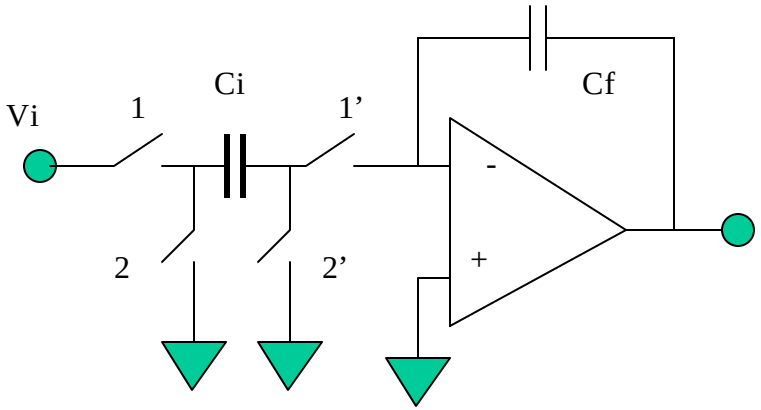
Is a matter of impedances



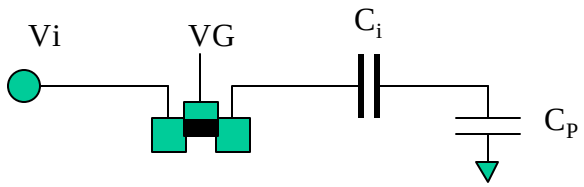
| If CP is small, then few electrons charge the capacitor at lower voltage, then rejecting the electrons. Then most of the charge is absorbed by the previous stage.

| IMPLEMENTATION?

Minimization of Clock Feedthrough



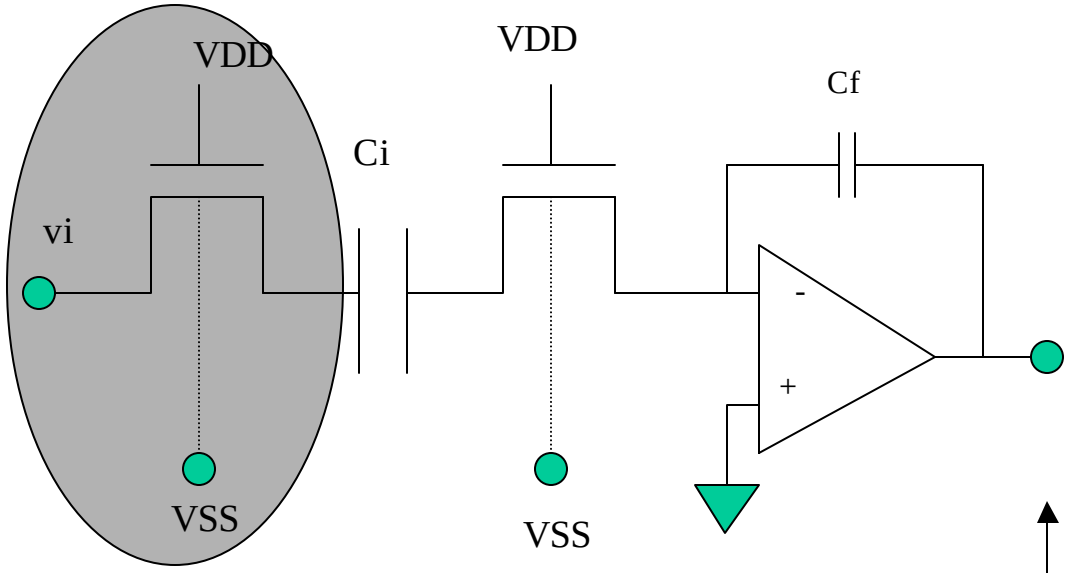
| The right hand side switches are opened before the others



| The equivalent capacitor is almost the parasitic.

| Error is minimized

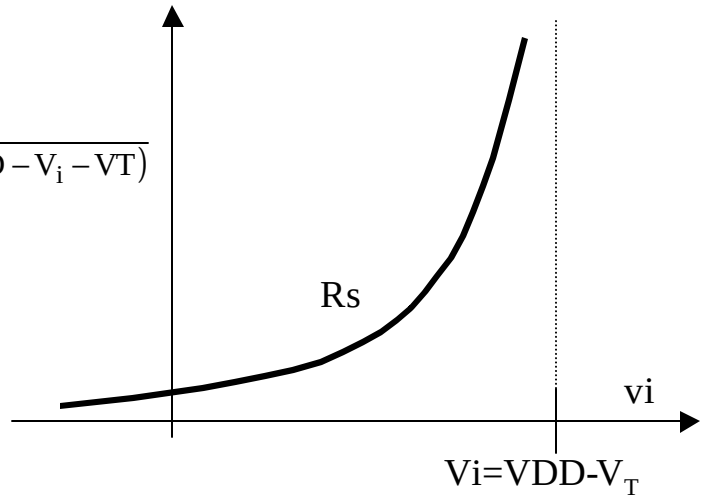
Switch Resistance



Body effect

$V_T=V_{T0}+\Delta V$

$$Rs=\frac{L}{\mu_n C_{OX} W(VDD-V_i-VT)}$$



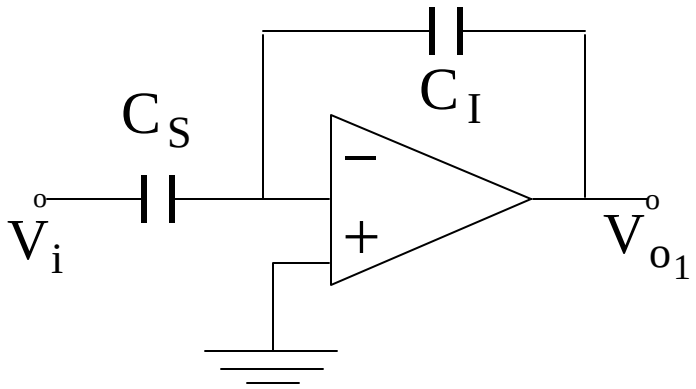
For VDD=1.5 V, and V_T=1 ==> Vi<0.5 V !!!

And for VDD=0.75 V ?

BASIC BUILDING BLOCKS

A. GAIN AMPLIFIERS

Basic Configuration:

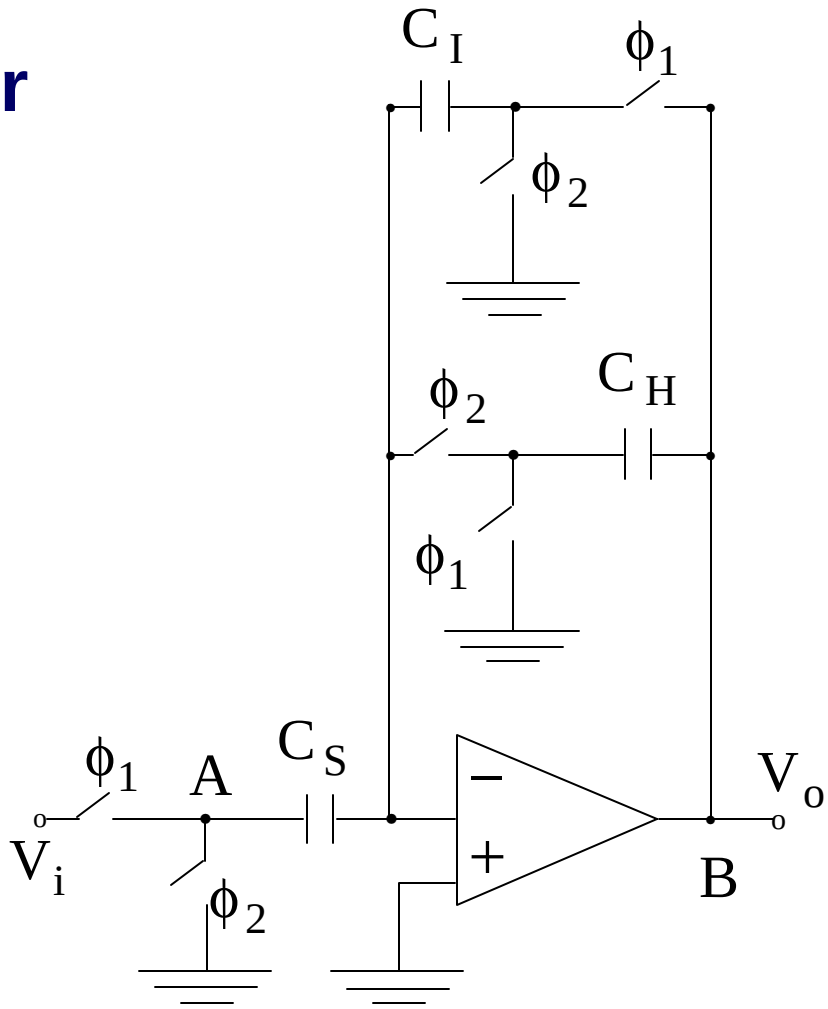


- Compact, versatile & time continuous
- Lacks dc feedback
  - Op amp is not stabilized
  - Leakage current saturates the circuit

$$\text{Gain} = -\frac{C_S}{C_I}$$

Improved Gain Amplifier

- Low sensitivity to the op amp offset voltage and open loop gain (due to charge cancellation
- Additional capacitor between nodes A and B eliminates the "spikes" during the non-overlapping clock phases

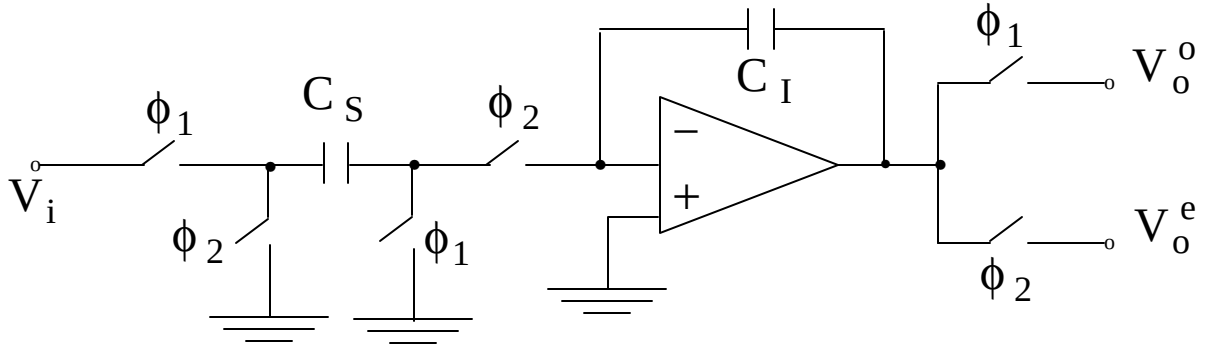


$$\text{gain} = -\frac{C_S}{C_I}$$

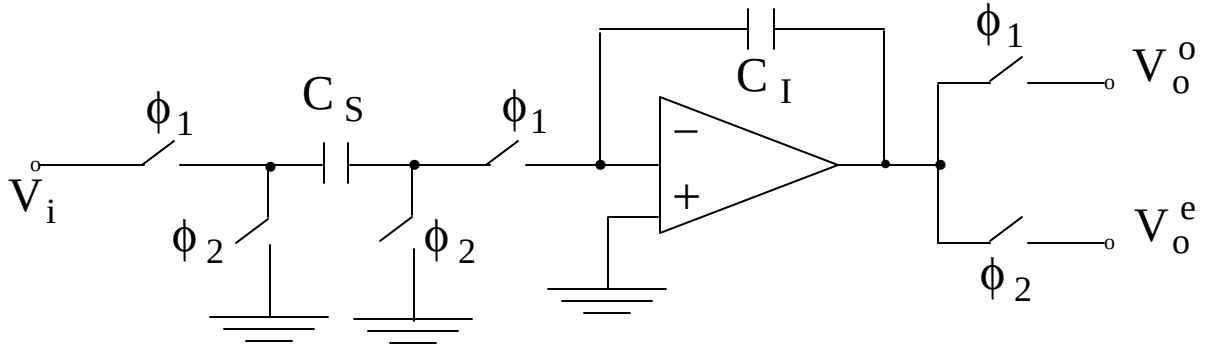
B. Integrators

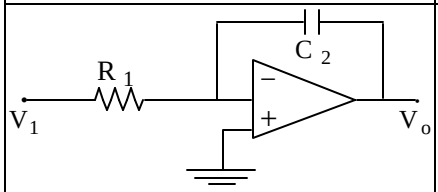
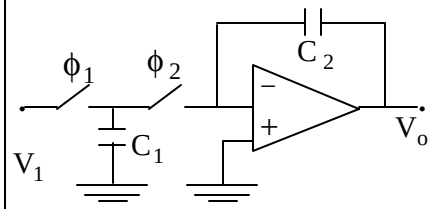
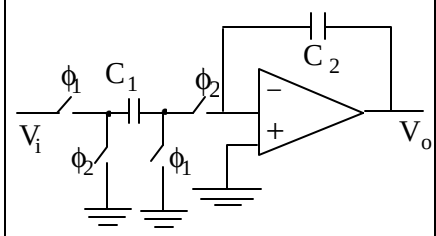
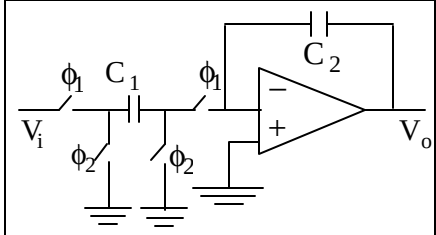
Conventional stray-insensitive integrators:

- Non-inverting:

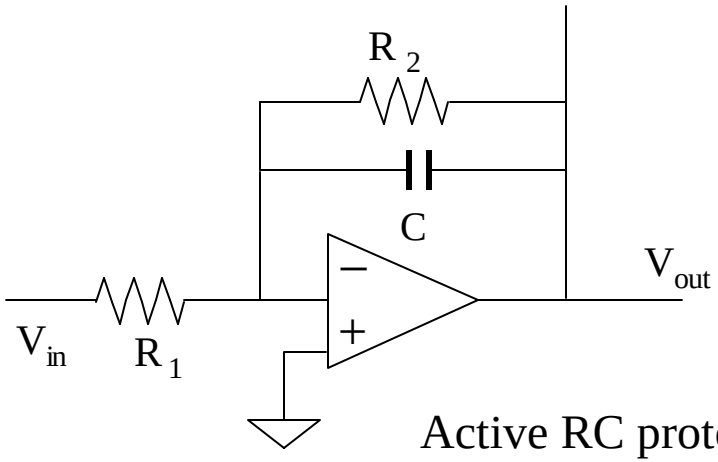


- Inverting:



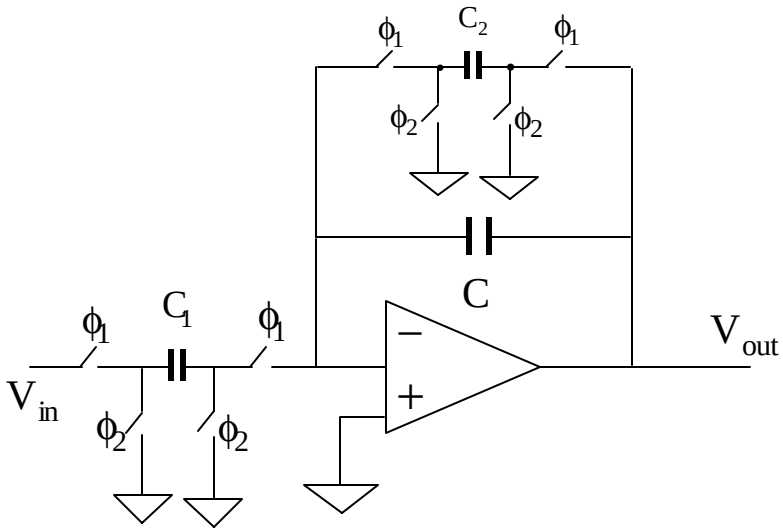
Type of Integrator	Magnitude, $\left\|H(e^{j\omega T})\right\|$	Phase, $A_{RG}H(e^{j\omega T})$	Mapping (Equivalent)	Transfer Function
	$\frac{\omega_o}{\omega}$	$\frac{\pi}{2}$	In the S-Plane	i.e. $H(S)=\frac{1}{SR_1C_2}=-\frac{\omega_o}{S}$
 Inverting (Forward)	For V_o at ϕ_2 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}$	LDI	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1/2}}{1-Z^{-1}}\right)$
	For V_o at ϕ_1 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}-\frac{\omega T}{2}$	Forward	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1}}{1-Z^{-1}}\right)$
 Non-Inverting	For V_o at ϕ_2 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$-\frac{\pi}{2}$	LDI	$H(Z)=\frac{C_1}{C_2}\left(\frac{Z^{-1/2}}{1-Z^{-1}}\right)$
	For V_o at ϕ_1 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$-\frac{\pi}{2}-\frac{\omega T}{2}$	Forward	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1}}{a-Z^{-1}}\right)$
 Inverting (Backward)	For V_o at ϕ_2 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}+\frac{\omega T}{2}$	Backward	$H(Z)=-\frac{C_1}{C_2}\left(\frac{1}{1-Z^{-1}}\right)$
	For V_o at ϕ_1 $\frac{\omega_o}{\omega}\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)$	$\frac{\pi}{2}$	LDI	$H(Z)=-\frac{C_1}{C_2}\left(\frac{Z^{-1/2}}{1-Z^{-1}}\right)$

Basic SC first-order low-pass



Active RC prototype

$$H(s) = \frac{-R_2/R_1}{1+sCR_2}$$



$$R_{eq} = T/C_i = 1/C_i f_S\ ,\ i = 1,2$$

$$H(z) = \frac{-(C_1/C)z}{z(1+C_2/C)-1}$$

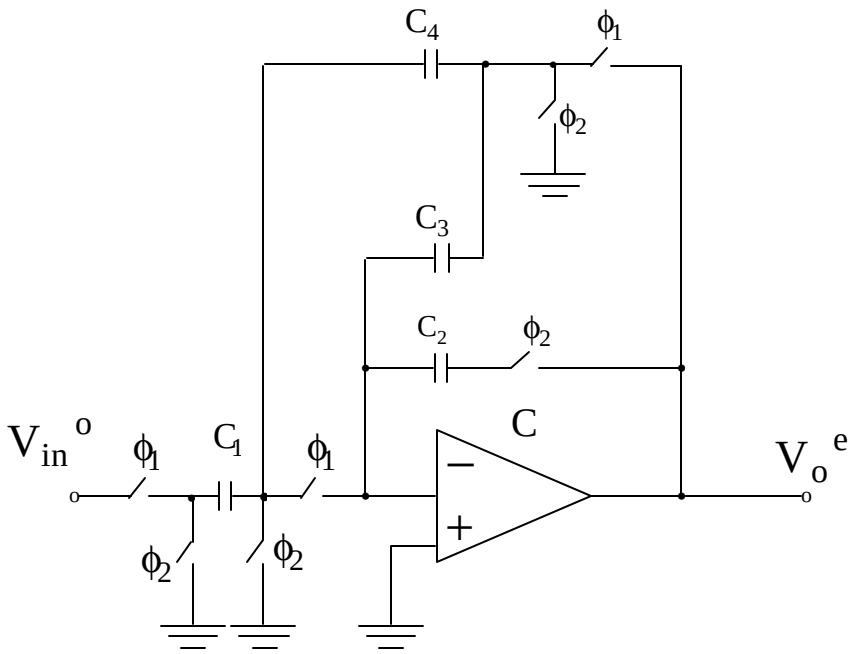
$$Z_{zero} = 0$$

$$Z_{pole} = 1/(1+C_2/C)$$

Improved Integrator with reduced capacitance spread

Problem: offset

Solution: use an offset & low dc gain compensated integrator as the 2nd stage (only valid for two-integrator loop applications)

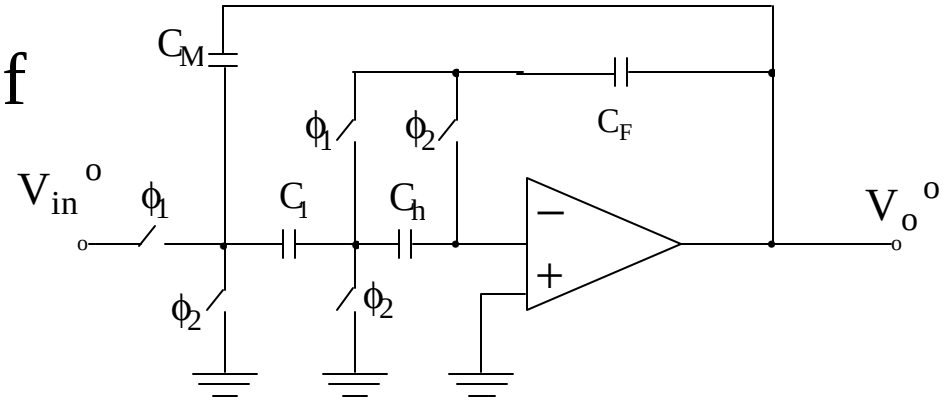


$$H^{oe}(z) = \frac{V_o^e(z)}{V_{in}^o(z)} = -\frac{C_1 C_3}{C_2 C_4^{'}} \frac{1}{1 - z^{-1}}$$

$$C_4^{'} = C_4 + C_3$$

Offset and gain compensated Integrator

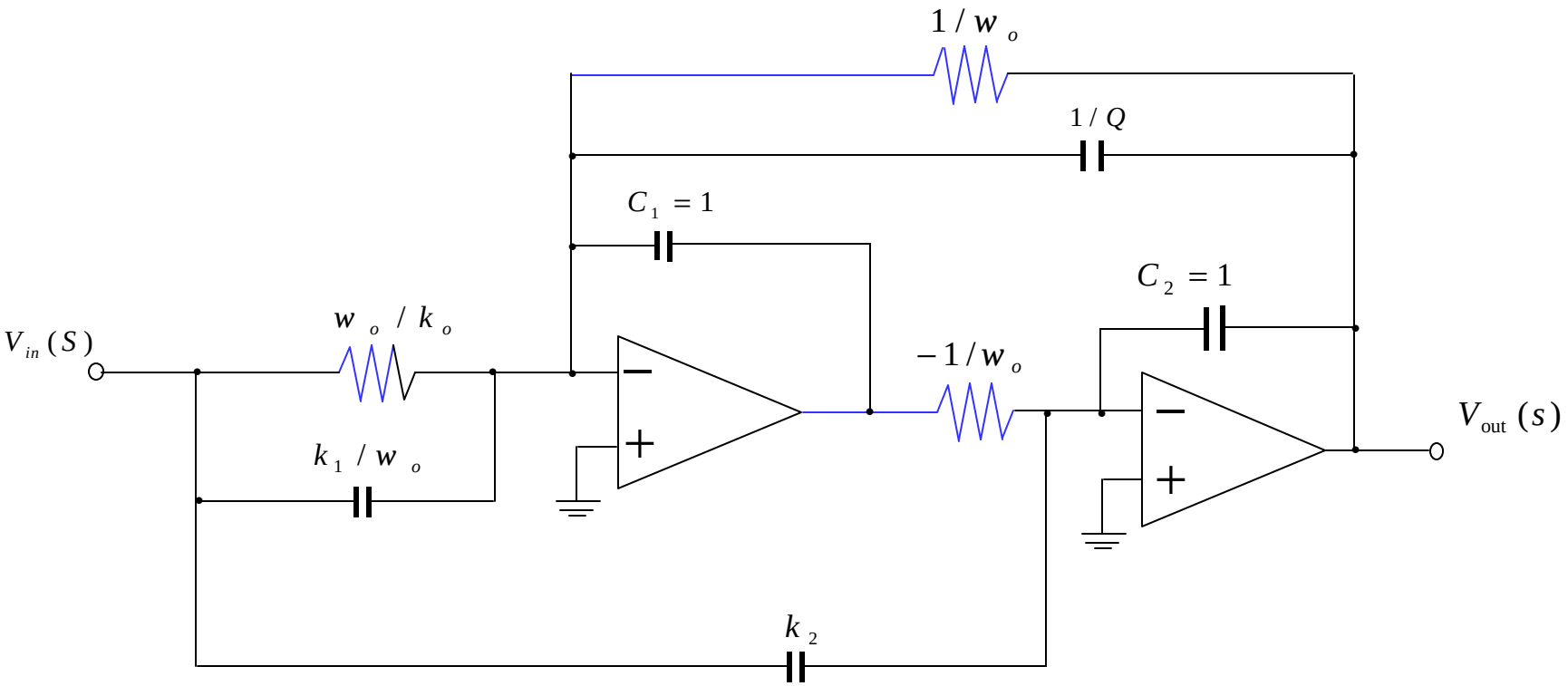
- C_h compensates the offset voltage and dc gain error of the op amp
- C_M eliminates spikes (providing continuous feedback to the op amp)



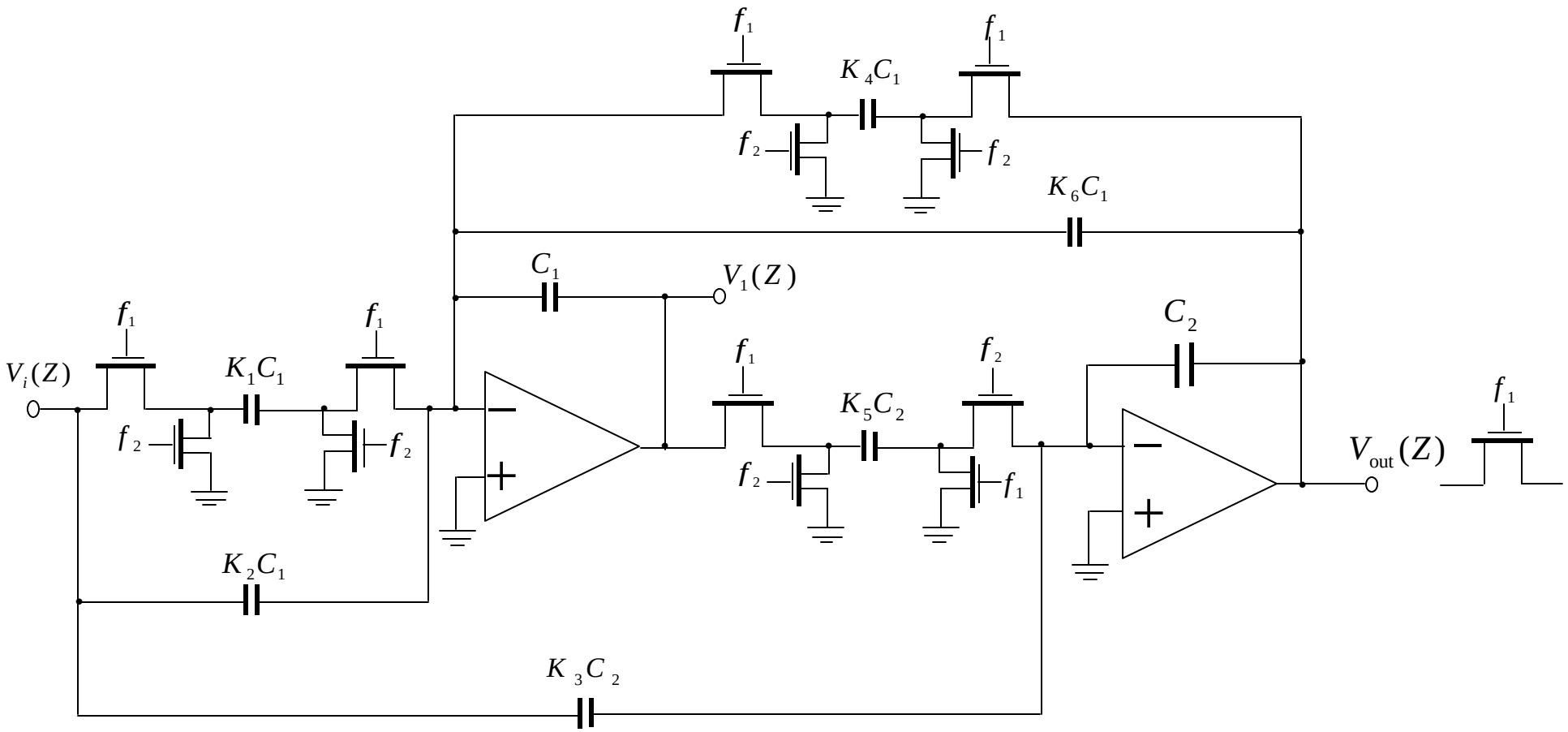
$$H^{oo}(z) = \frac{V_o^o(z)}{V_{in}^o(z)} = -\frac{C_1}{C_F}\frac{1}{1-z^{-1}}$$

A direct mapping from an active-RC filter into a SC Filter.

Since negative (equivalent) resistances are easily implemented in SC,
a modified Active-RC prototype is next described



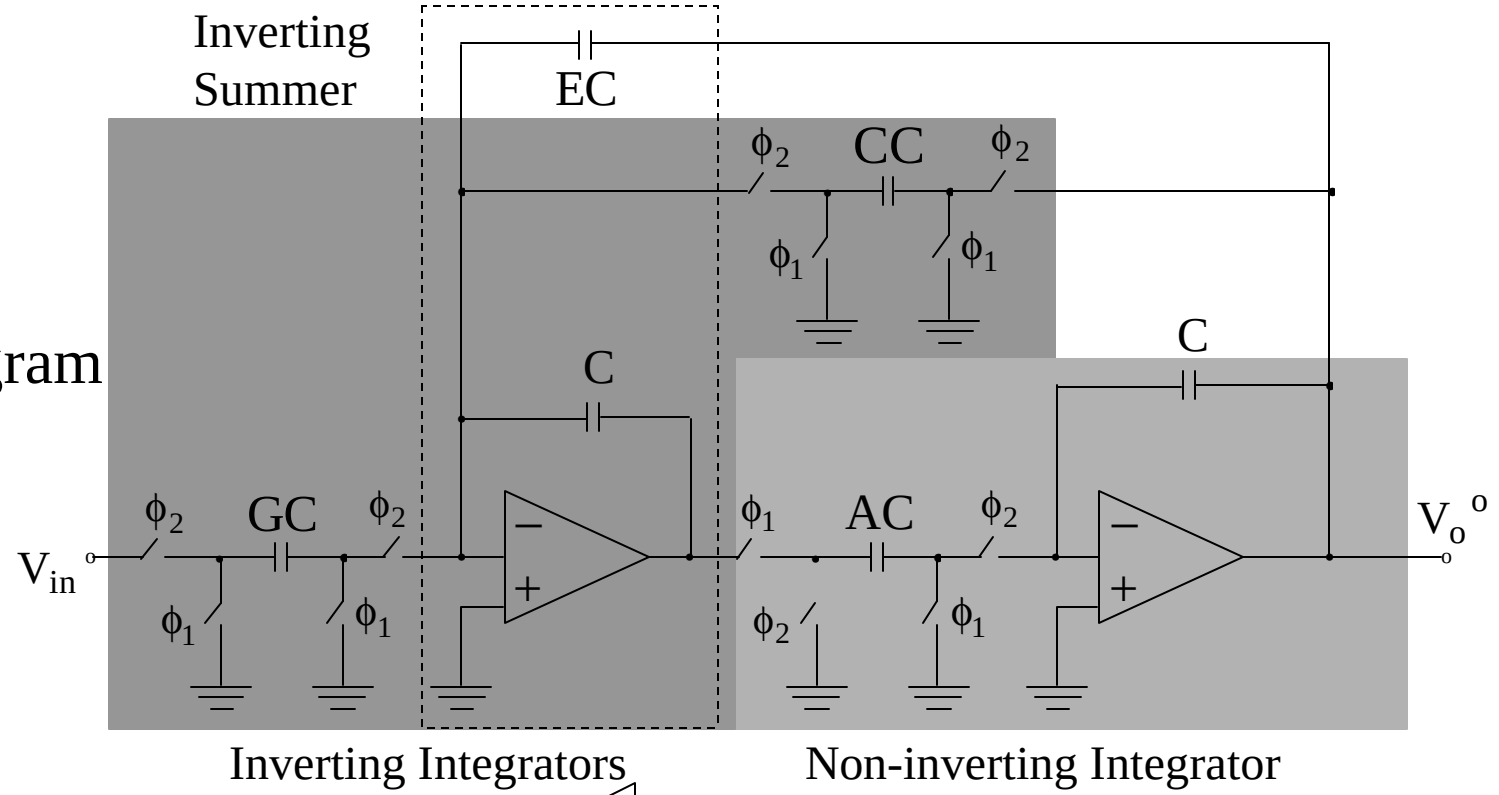
An alternate realization of a general active-RC biquad filter



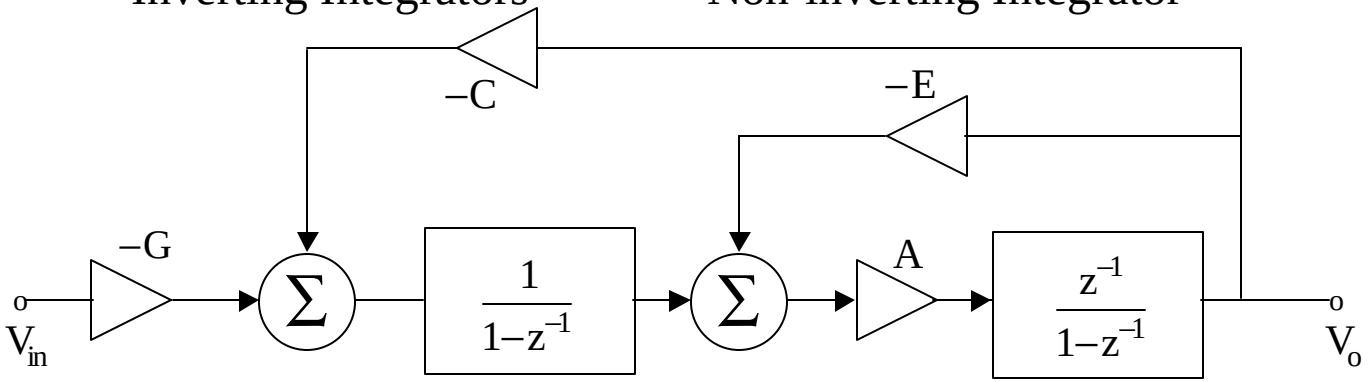
A high-Q switched-capacitor biquad filter (without switch sharing).

Biquad Circuit & Block Diagrams

Circuit Diagram

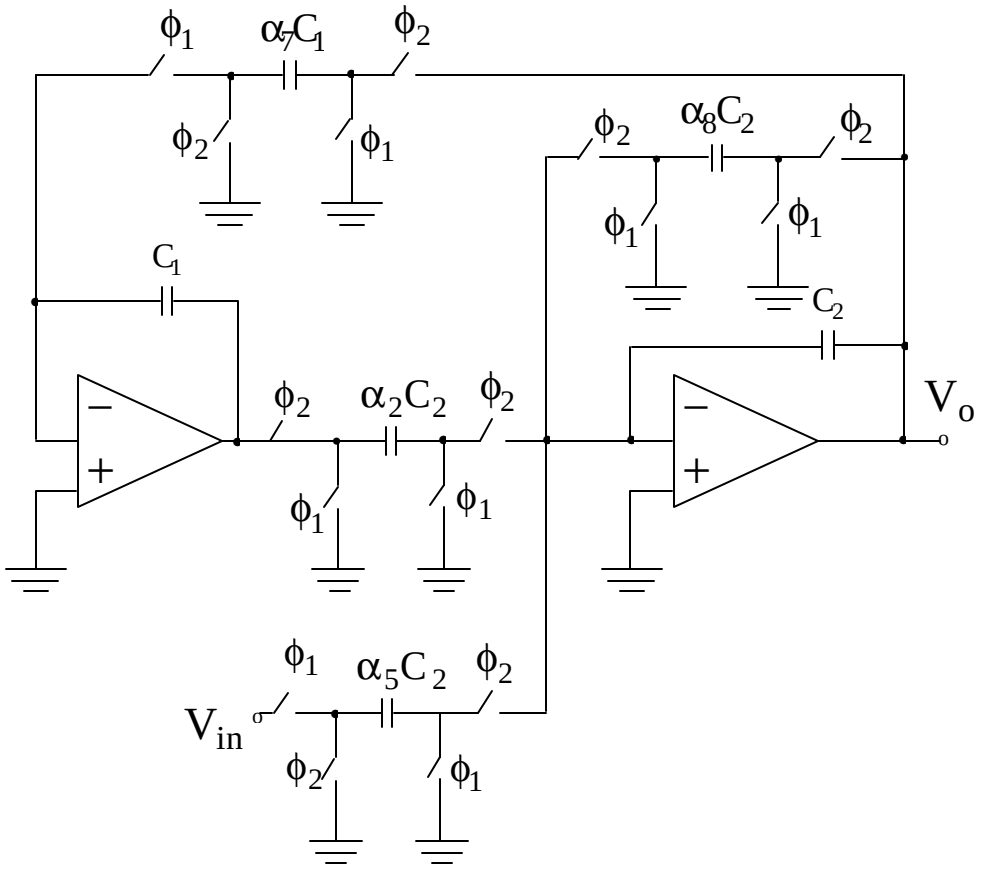


Block Diagram



Biquad Circuit 1

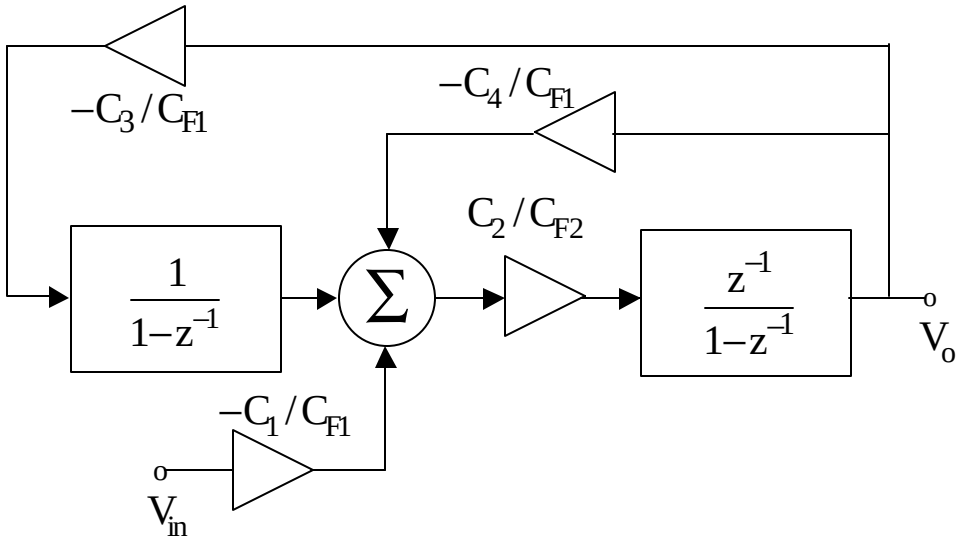
Circuit Diagram



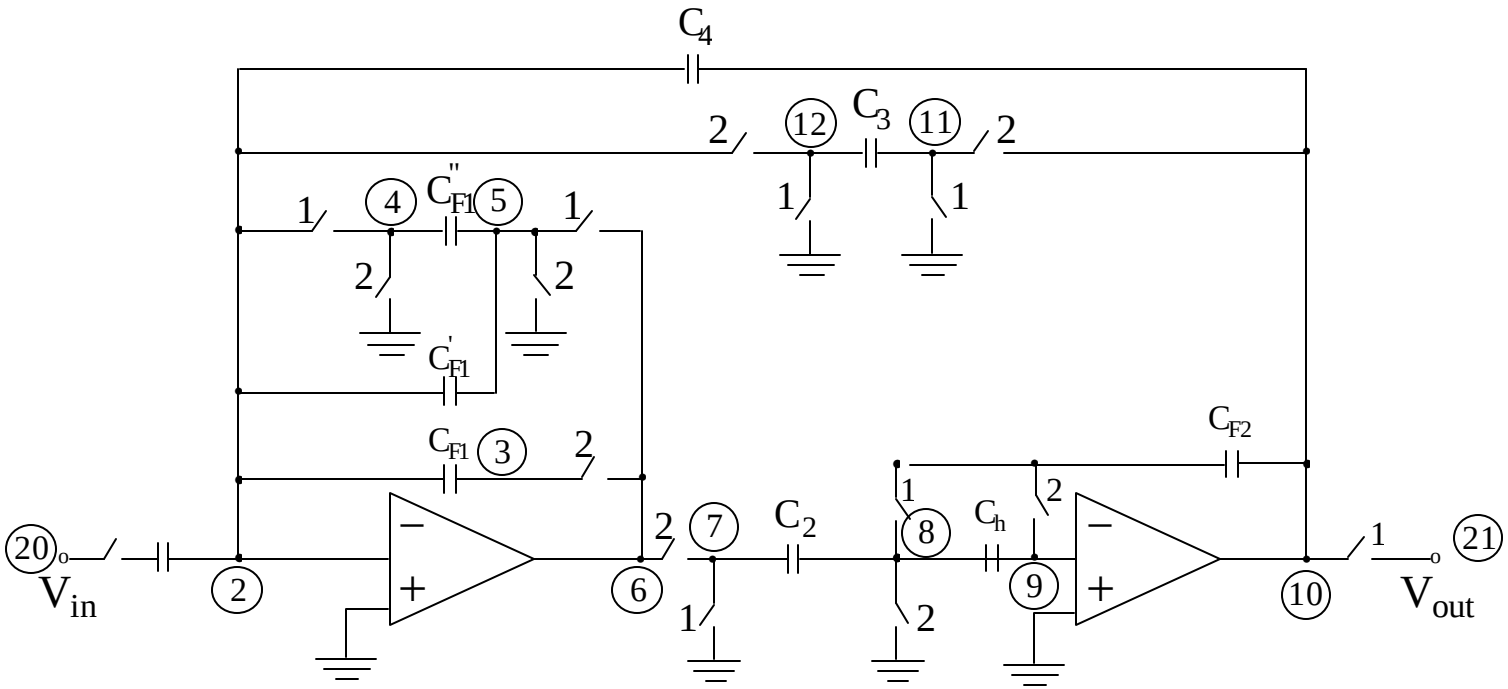
Block Diagram

Biquad Circuit 2

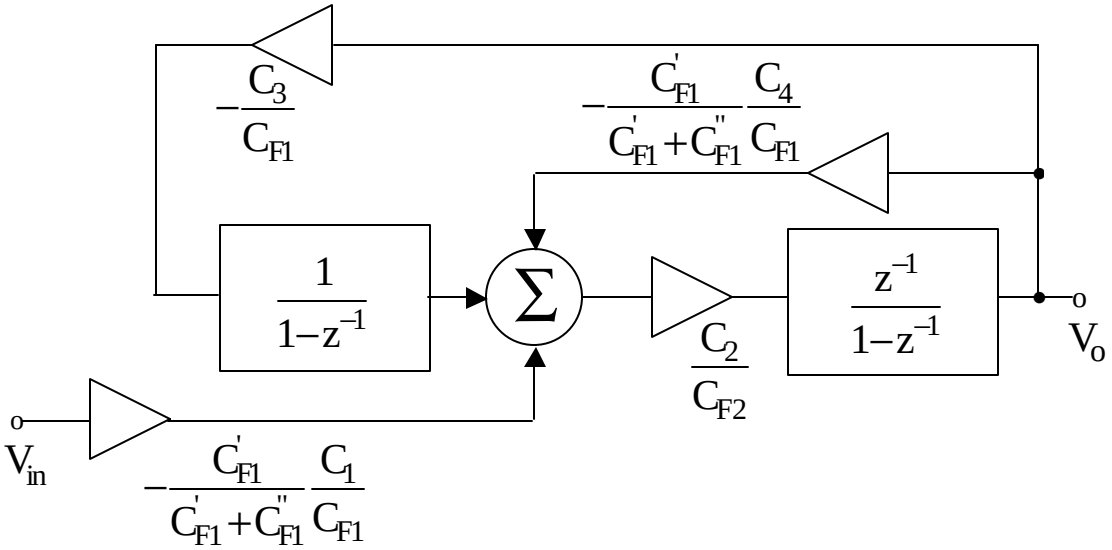
Block Diagram



Circuit Diagram



SC Bandpass C Diagram



SC Bandpass Filter Block Diagram

Capacitor Values for the SC Filter

Capacitor Values		
f_o(Hz)	C'_{F1}(Cu)	$C_{F1} = C_{F2}$(Cu)
697	4	11.4
852	2.6	9.3
1209	1.5	6.6
1477	1.1	5.4
Where: $C_2 = C_3 = C_4 = C_h = 1\,\text{Cu}$, $C_1 = 2.2\,\text{Cu}$, $C''_{F1} = 3\,\text{Cu}$ and $f_c = 1/T = 50\,\text{kHz}$		

Specifications vs. Simulated Results for the SC Filter

Design Specifications			Simulated Results		
Gain (v/v)	f_o(Hz)	Q	Gain (v/v)	f_o(Hz)	Q
1	697	20	0.998	699.00	19.92
1	852	20	0.999	857.25	20.02
1	1209	20	1.000	1209.00	19.83
1	1477	20	1.002	1479.00	20.11

Design of 2nd-Order LP Notch Filter

Design a LP Notch Filter with f_z=1,800 Hz, f_p= 1,700 Hz, Q_p=30 and 0dB DC Gain.
The corresponding H(s) yields:

$$H(s) = \frac{0.89195\,s^2 + (1.140926 \times 10^8)}{s^2 + 356.0475\,s + (1.140926 \times 10^8)}$$

By using the bilinear mapping

$$s = K\frac{1 - z^{-1}}{1 + z^{-1}}$$

where $K = \omega a / \tan(\omega_d T/2)$

The corresponding transfer function becomes:

$$H(z) = 0.89093\,\frac{1 + 1.99220\,z^{-1} + z^{-2}}{1 - 1.99029\,z^{-1} + 0.997232\,z^{-2}}$$

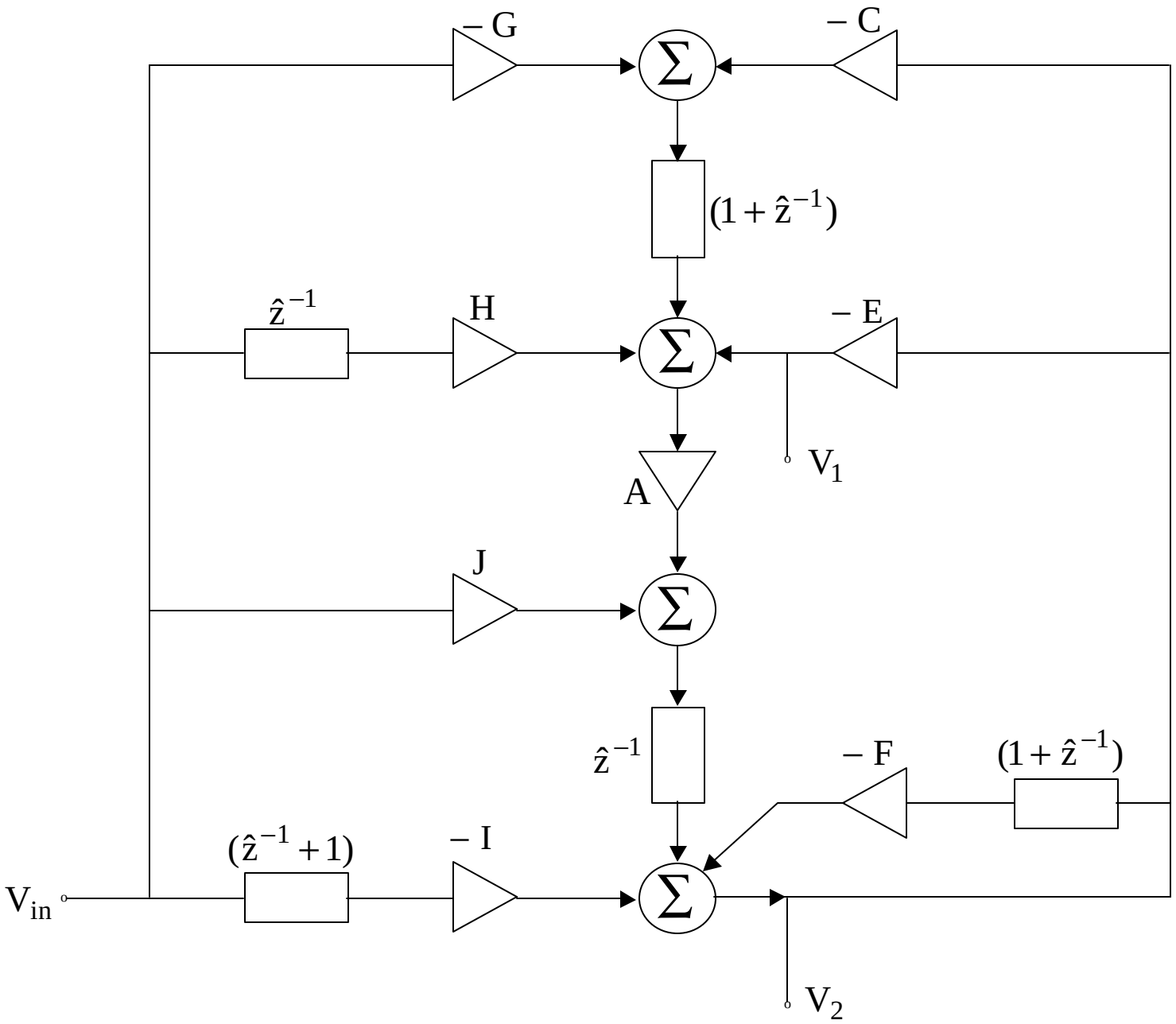
Next we will match the coefficients of H(z) with the ones of a SC Biquad Topology, i.e.,

$$H_{E_z}(\hat{z}) = -\frac{I + (I + G - J)\hat{z}^{-1} + (G - H)\hat{z}^{-2}}{1 + (E + C)\hat{z}^{-1} + C\hat{z}^{-2}}$$

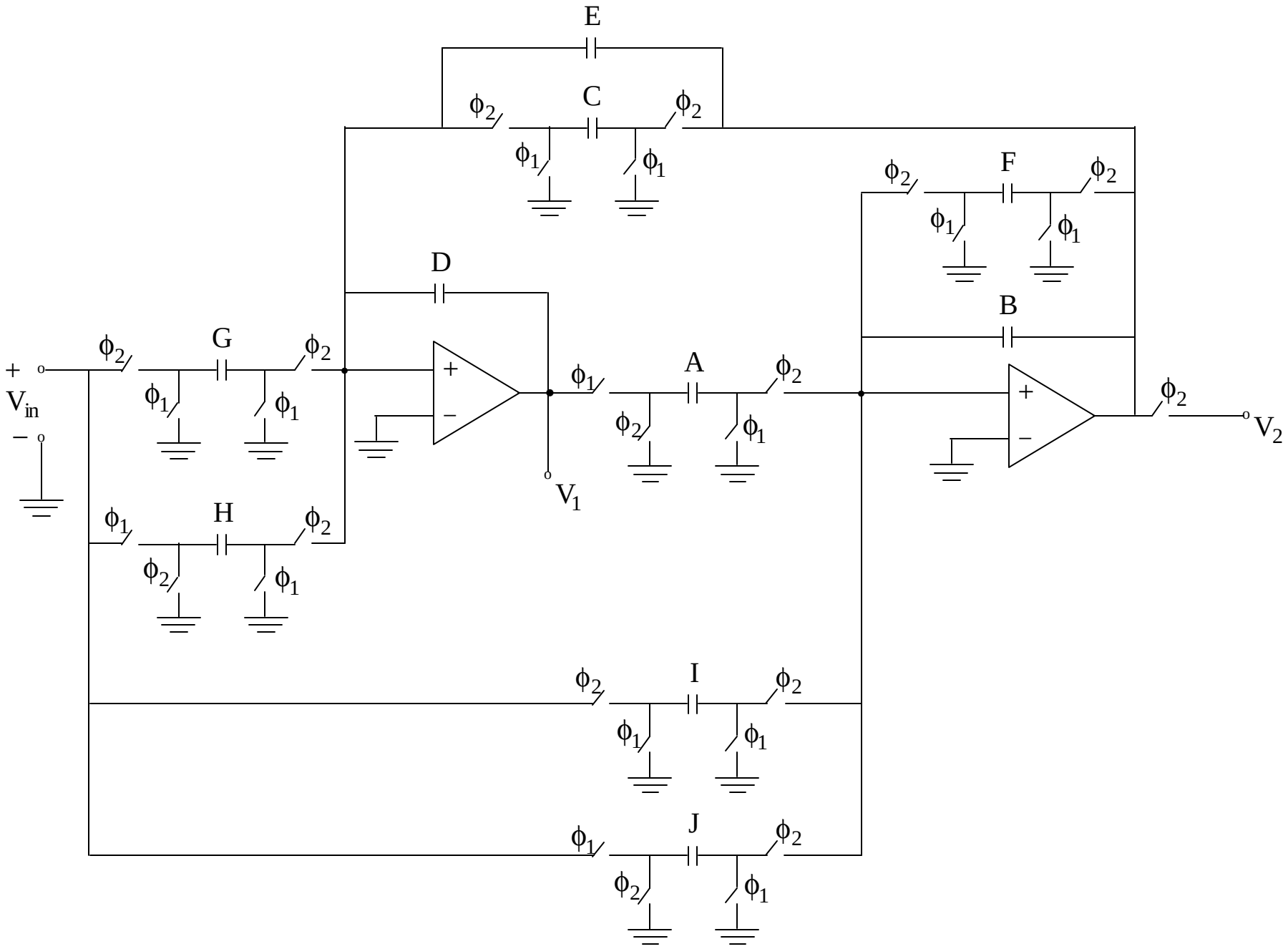
where $\hat{z}^{-1} = \dfrac{z^{-1}}{1 - z^{-1}}$; $\quad \hat{z} = z - 1$

$$H(\hat{z}) = 0.89093\,\frac{1 + 0.0078\,\hat{z}^{-1} + 0.0078\,\hat{z}^{-2}}{1 + 0.0097\,\hat{z}^{-1} + 0.000694\,\hat{z}^{-2}}$$

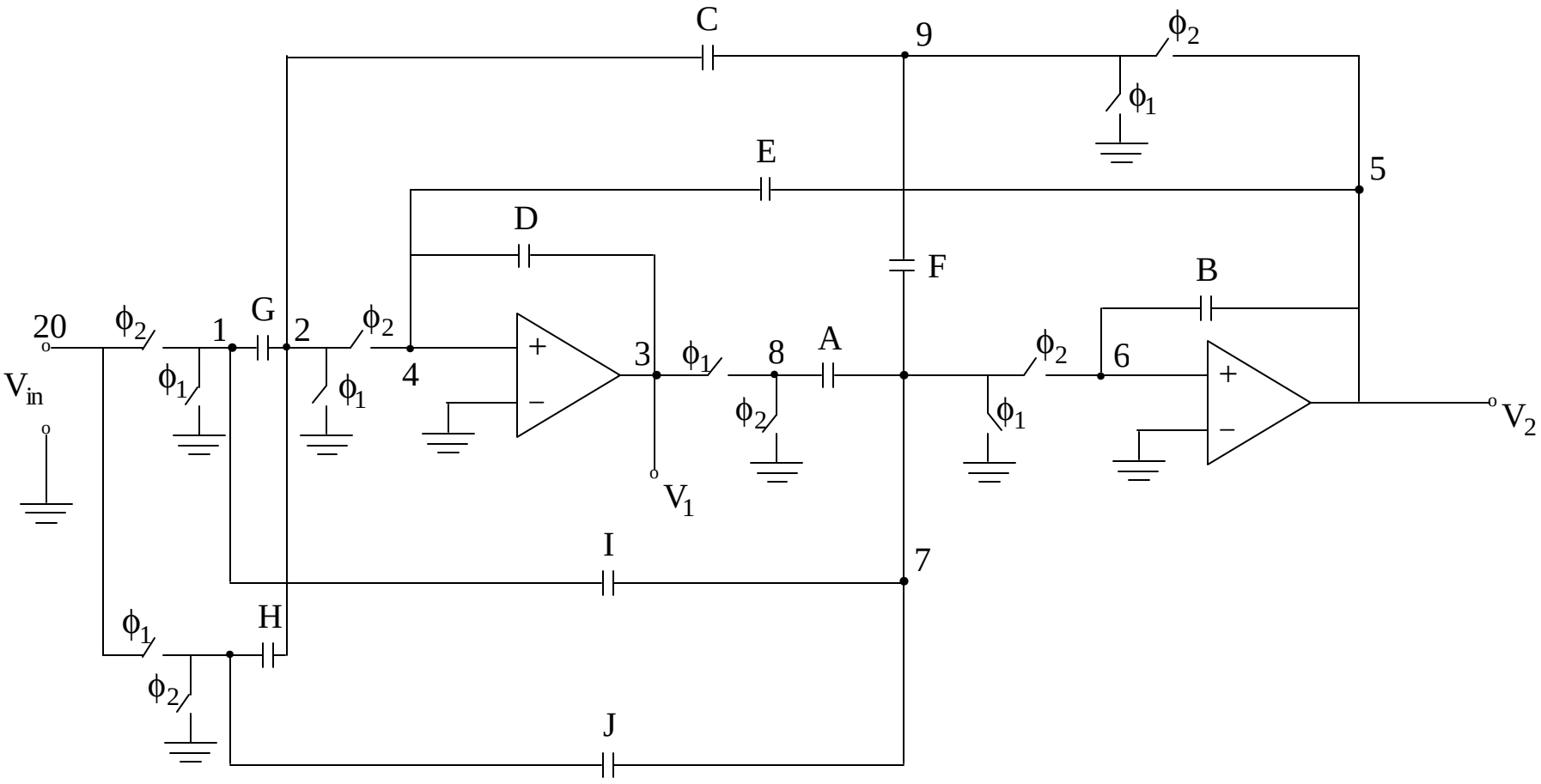
CAPACITOR (PF)	E-CIRCUIT		
	INITIAL	DYNAMIC RANGE ADJUSTED	FINAL
A	1.0000	0.08308	1.0000
B	1.0000	1.0000	12.0365
C	0.00694	0.00694	2.5035
D	1.0000	0.08308	29.9613
E	0.00277	0.00277	1.0000
F	---	---	---
G	0.00694	0.00694	2.5035
H	---	---	---
I	---	---	---
J	---	---	---
K(I=J)	0.89093	0.89093	10.7238
$\sum$ C(pF)	---	---	59.7



A general SC biquad flow diagram type 1.



SC implementation with maximum number of switches.

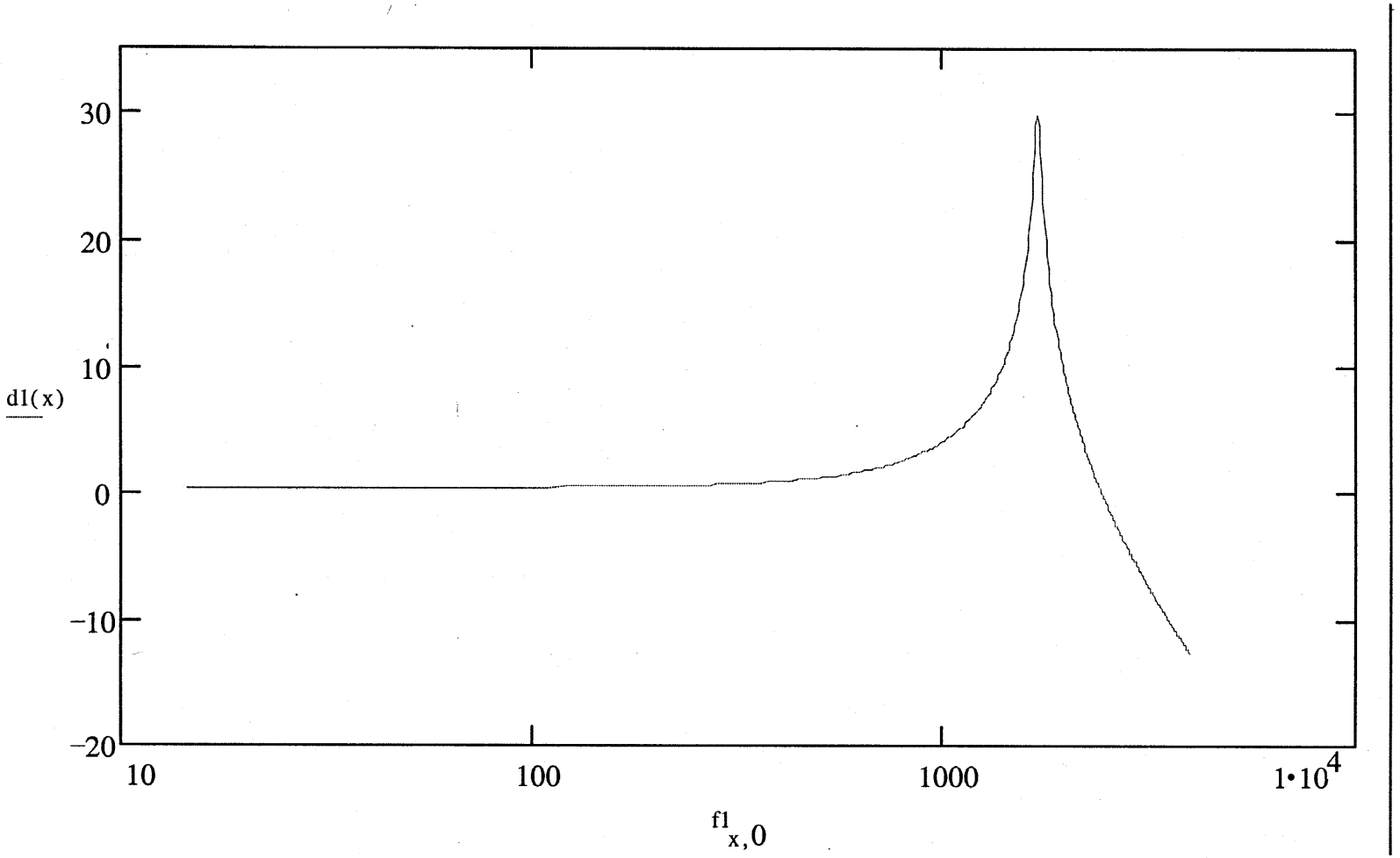


SC implementation minimum switch configuration.

SWITCAP Input file

```
timing;
period 7.8125e-06;
clock clk 1 (0 1/2);
end;

circuit;
cg   (1 2) 2.5935;
ca   (8 7) 1.0000;
cd   (4 3) 29.9613;
cb   (6 5) 12.0365;
ce   (4 5) 1.00000;
cc   (2 9) 2.5035;
e1   (3 0 0 4) 28000;
e2   (5 0 0 6) 28000;
s1   (20 1) #clk;
s4   (2 4) #clk;
s5   (9 5) #clk;
s9   (8 0) #clk;
s10  (7 6) #clk;
s2   (1 0) clk;
s3   (2 0) clk;
s6   (9 0) clk;
s7   (3 8) clk;
s8   (7 0) clk;
v1   (20 0);
end;
analyze sss;
infreq 1 4000 lin 300;
set v1 ac 1.0 0.0;
print vm(5);
plot vm(5);
```

Low-pass notch SC



f_p = 1,700 Hz, f_z =1,800 Hz, Qp = 30, DC Gain = 0 dB

Periodic Non-Uniform Switched-Capacitor Technique

Francisco Duque-Carrillo & Edgar Sánchez-Sinencio

- Switched-capacitor techniques conventionally have only two degrees of freedom:
  - clock frequency
  - capacitor ratios

i.e.,

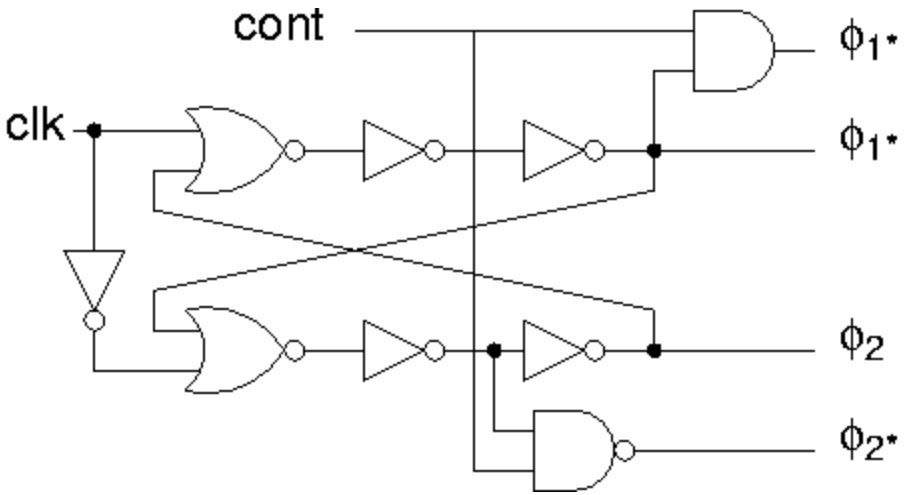
$$t = R_{eq}C = \frac{T_s \cdot C}{C_{eq}} = \frac{1}{f_s} \cdot \frac{C}{C_{eq}}$$

Different values for Ceq can be realized to achieve different time constants by employing capacitor arrays at the cost of:

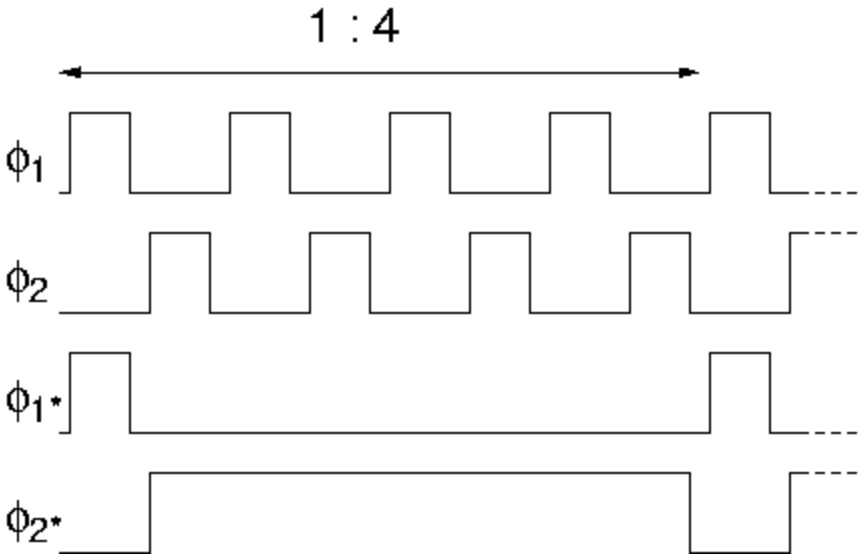
- increased silicon area consumption,
- reduced accuracy due to nonlinear parasitics associated with a large number of switches.

Instead one can use the recently introduced *periodically nonuniform individual sampling* technique. In this technique, one can mask the main clock controlling certain switches to program parameters such as gain, center frequency, and quality factor.

Generating auxiliary clock waveforms

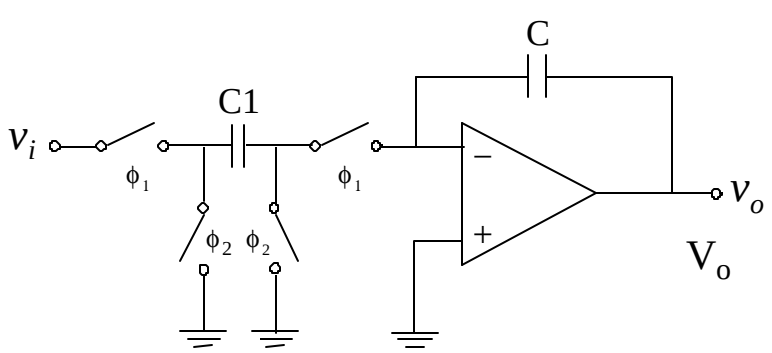


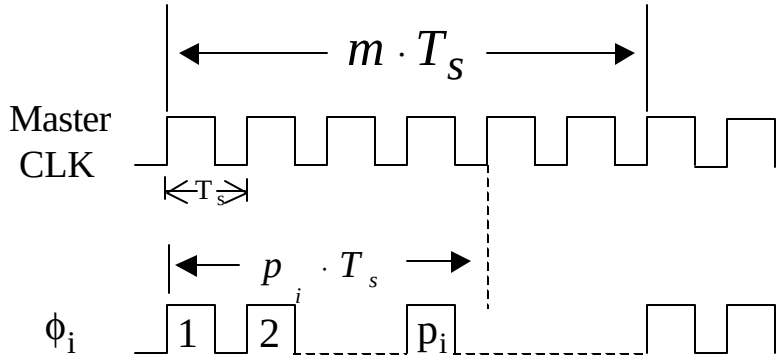
Example (m=4, p=1)



Periodic Non-Uniform Switched Capacitor Principle

- The number of active pulses (p_i) of a switched-capacitor branch controls the equivalent resistance value.



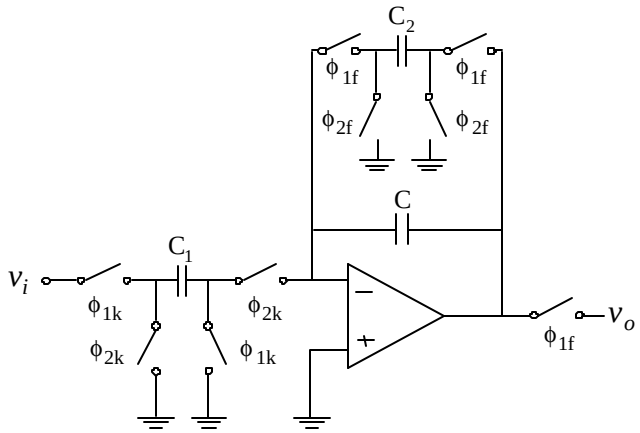


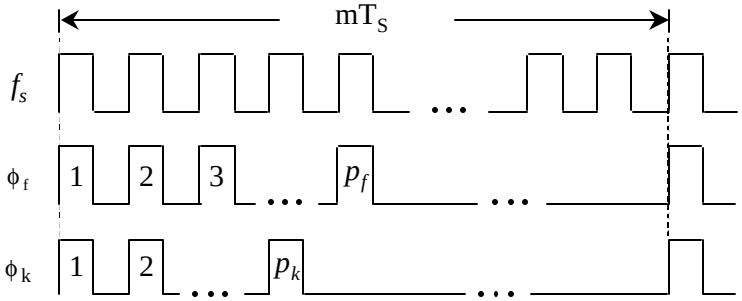
$$t = R_{eq} \cdot C = \frac{m}{p_i} \cdot \left(\frac{T_s \cdot C}{C_1} \right)$$

An additional degree of freedom (m/p_i) is provided by this approach

Periodic Non-Uniform Switched-Capacitor Example

- In more complex switched-capacitor networks, any response parameter can be fully-programmed by means of the number of active pulses of some switched-capacitor branches:





- DC gain:

$$H(0) = \frac{p_k}{p_f} \cdot \frac{C_1}{C_2}$$

- Cutoff frequency (w_o):

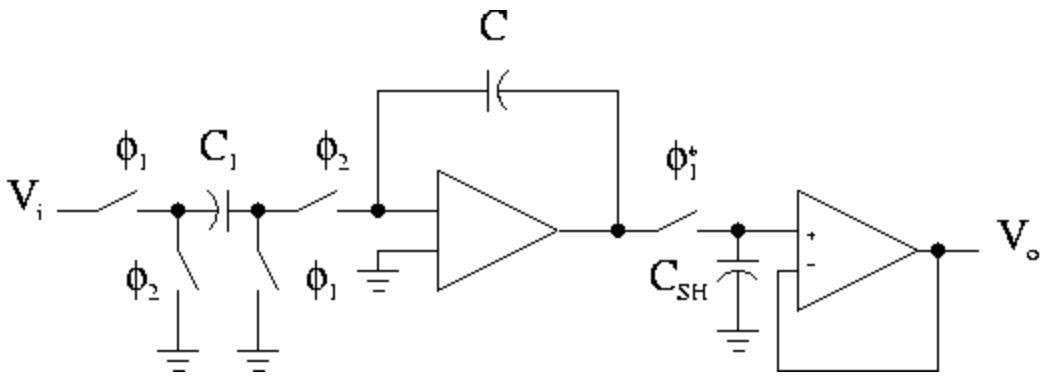
$$z = e^{jw_o mT_s} = \left(\frac{C}{C + C_2} \right)^{p_f}$$

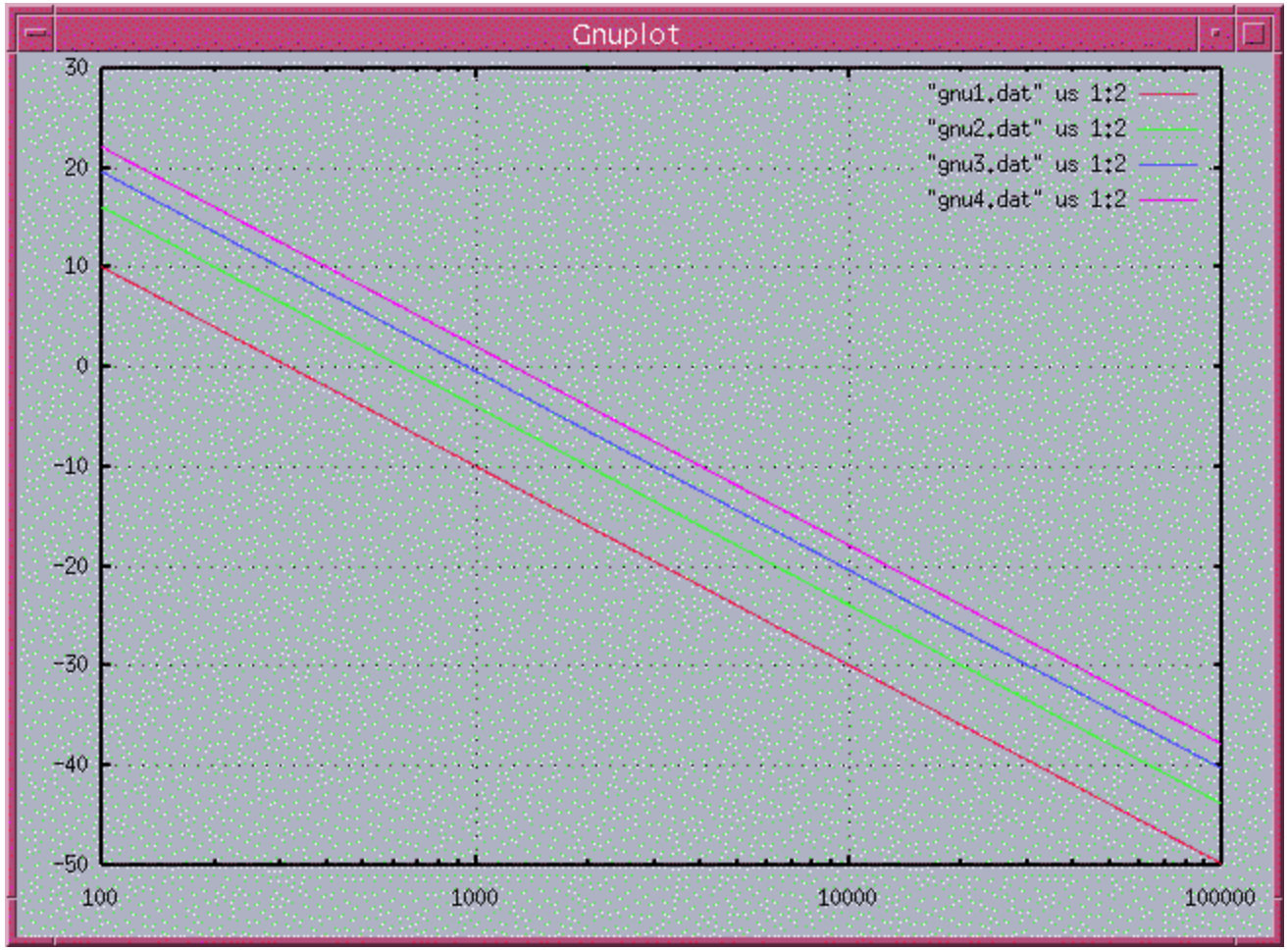
SIMULATIONS USING SWITCAP

Example 1: Noninverting switched-capacitor integrator: programming unity gain frequency

$$|H(z)| = \frac{1}{wT_s}\frac{p}{m}\frac{C_1}{C}\frac{1}{\sin c(wT_s/2)}\frac{\sin c(pwT_s/2)}{\sin c(mwT_s/2)}$$

$$w_0 = \frac{1}{T_s}\frac{p}{m}\frac{C_1}{C}$$


C
ϕ_1
C_1
ϕ_2
ϕ_1^*
V_i
V_o
ϕ_2
ϕ_1
C_{SH}

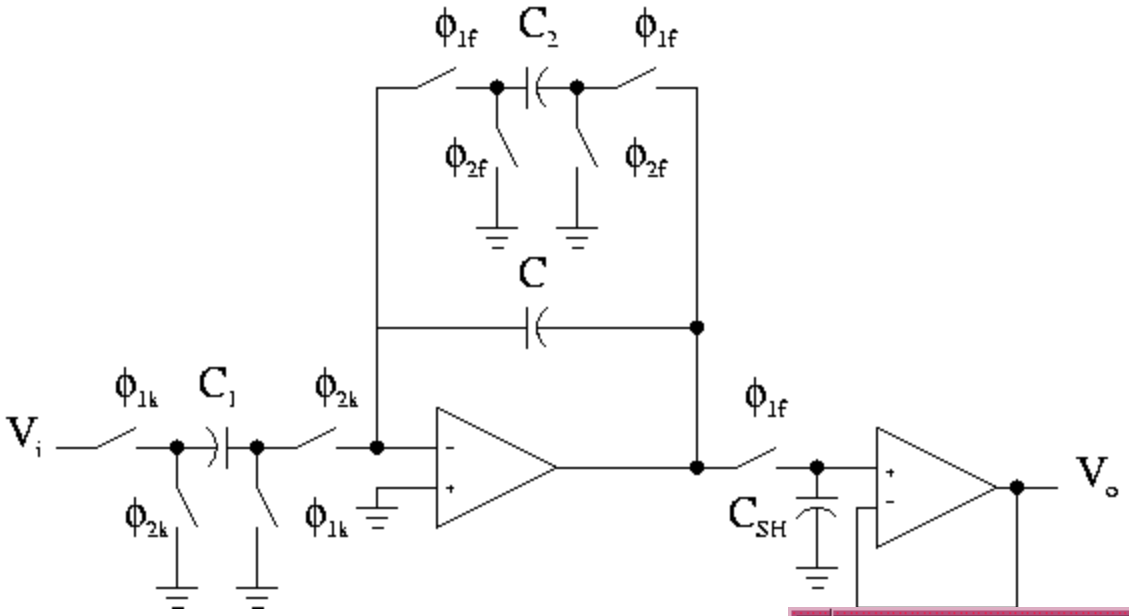

Gnuplot
"gnu1.dat" us 1:2
"gnu2.dat" us 1:2
"gnu3.dat" us 1:2
"gnu4.dat" us 1:2
30
20
10
0
-10
-20
-30
-40
-50
100
1000
10000
100000

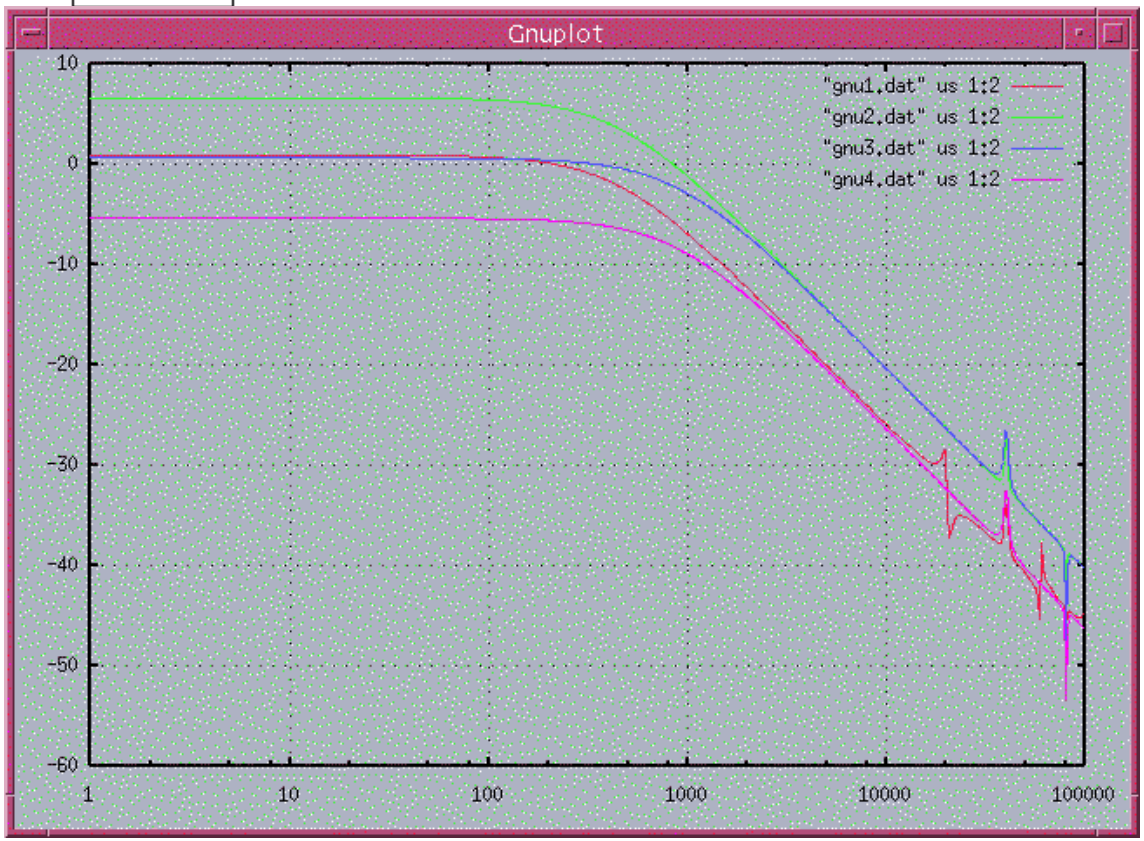
```
title: noninverting integrator
timing;
               period 25e-6;
/*  p = 1 */
/*        clock phi1 4 (0 1/2);  */

/*  p = 2 */
/*      clock phi1 4 (0 1/2) (2/2 3/2);    */

/*  p = 3 */
/*      clock phi1 4 (0 1/2) (2/2 3/2) (4/2 5/2);  */

/*  p = 4 */
      clock phi1 4 (0 1/2) (2/2 3/2) (4/2 5/2) (6/2 7/2);


        clock phiSH 4 (0 1/2);
end;


subckt (1 4) DlessRes (K:phi P:cap1);

               s1 ( 1 2 ) phi;
               s2 ( 2 0 ) #phi;
               s3 ( 3 4 ) phi;
               s4 ( 3 0 ) #phi;
               c1 ( 3 2 ) cap1;

end;


subckt (1 4) DNegRes (K:phi P:cap2);

               s1 ( 1 2 ) phi;
               s2 ( 2 0 ) #phi;
               s3 ( 3 4 ) #phi;
               s4 ( 3 0 ) phi;
               c2 ( 3 2 ) cap2;
end;



subckt (1 2) ActCap (P:gain P:capA);

               e1 ( 2 0 0 1 ) gain;
               ca ( 1 2) capA;

end;
```

```
subckt (1 3) SampleHold(K:phi P:gain P:capSH);

        s1 (1 2) phi;
        e1 (3 0 2 3) gain;
        c1 (2 0) capSH;

end;


circuit;
               V1 (1 0);
               X1 (1 2) DNegRes (phi1 0.4);
               X2 (2 3) ActCap (1e9 2);
        X3 (3 4) SampleHold (phiSH 1e9 1);
end;



analyze sss;

               infreq 1e+2 1e+5 log 1000;
               set V1 ac 1.0 0.0;
               print vdb(3) vdb(4);

end;


/*
analyze tran;
               time 0+ 40 1/4;
               set V1 cosine 0 3 10e3 0 0 0;
               sample input hold  1 4/8+;
/*             sample output hold 1 4/8-; */
               print v(3) v(4);
end;
*/



end;
```

Ex 2: Noninverting damped switched-capacitor integrator: $a = C_1/(C + C_2)$

pk	pf	f(-3dB)	dc gain
1	1	$\exp(j2wT_s) = a$	$\frac{C_1}{C_2}$
2	1	$\exp(j2wT_s) = a$	$2\frac{C_1}{C_2}$
2	2	$\exp(jwT_s) = a$	$\frac{C_1}{C_2}$
1	2	$\exp(jwT_s) = a$	$\frac{1}{2}\frac{C_1}{C_2}$


ϕ_{1f}
C_2
ϕ_{1f}
ϕ_{2f}
ϕ_{2f}
C
ϕ_{1k}
C_1
ϕ_{2k}
V_i
ϕ_{2k}
ϕ_{1k}
ϕ_{1f}
C_{SH}
V_o

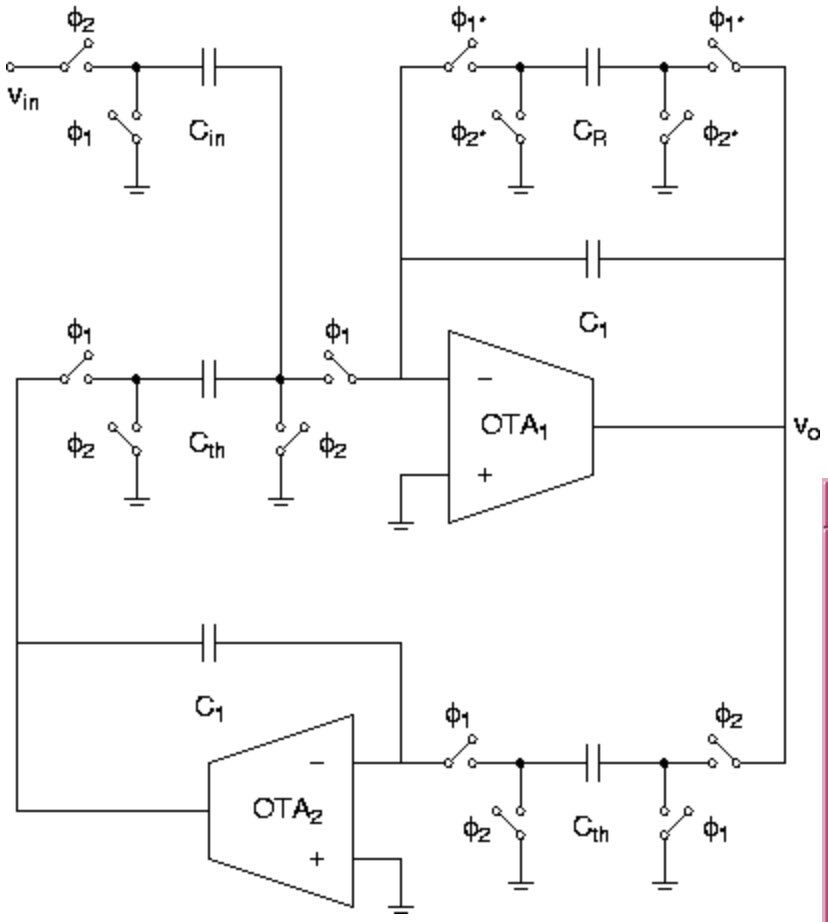

Gnuplot
"gnu1.dat" us 1:2
"gnu2.dat" us 1:2
"gnu3.dat" us 1:2
"gnu4.dat" us 1:2
10
0
-10
-20
-30
-40
-50
-60
1
10
100
1000
10000
100000

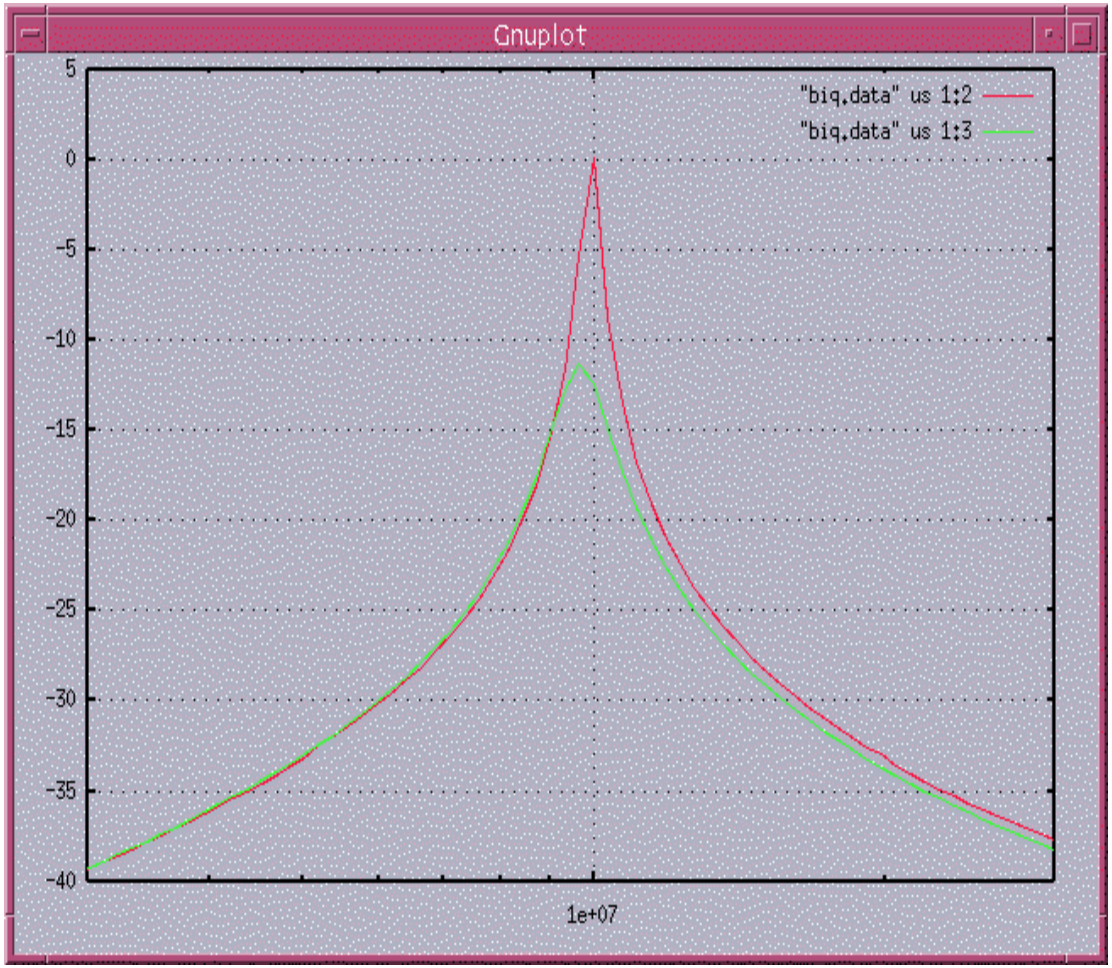
```
title: noninverting damped SC integrator
timing;
          period 25e-6;
/* master clock: m = 2   */
/* pk = 1 */
         clock pk 1 (0 1/2)
/* pk = 2 */
/*          clock pk 2 (0 1/2) (2/2 3/2); */
/* pf = 2 */
          clock pf 2 (0 1/2) (2/2 3/2);
end;

subckt (1 4) DlessRes (K:phi P:cap1);

          s1 ( 1 2 ) phi;
          s2 ( 2 0 ) #phi;
          s3 ( 3 4 ) phi;
          s4 ( 3 0 ) #phi;
          c1 ( 3 2 ) cap1;
end;

subckt (1 4) DNegRes (K:phi P:cap2);

          s1 ( 1 2 ) phi;
          s2 ( 2 0 ) #phi;
          s3 ( 3 4 ) #phi;
          s4 ( 3 0 ) phi;
          c2 ( 3 2 ) cap2;
end;

subckt (1 2) ActCap (P:gain P:capA);

          e1 ( 2 0 0 1 ) gain;
          ca ( 1 2) capA;
end;
```

```
subckt (1 3) SampleHold(K:phi P:gain P:capSH);

          s1 (1 2) phi;
          e1 (3 0 2 3) gain;
          c1 (2 0) capSH;
end;


circuit;
          V1 (1 0);
          X1 (1 2) DNegRes (pk 0.3);
          X2 (2 3) ActCap (1e9 2.0);
          X3 (2 3) DLessRes(pf 0.3)
          X4 (3 4) SampleHold (pf 1e9 1);
end;

analyze sss;
            infreq 1 1e+5 log 1000;
            set V1 ac 1.0 0.0;
            print vdb(3) vdb(4);
end;


end;
```

Ex ample 3: Biquadratic section: programming Q (N=4)

$$Q = N \frac{C_{th}}{C_R}$$


ϕ2
vin
ϕ1
Cin
ϕ1*
ϕ1*
ϕ2*
CR
ϕ2*
C1
ϕ1
ϕ1
ϕ2
Cth
ϕ2
OTA1
vo
C1
OTA2
ϕ1
ϕ2
ϕ2
Cth
ϕ1

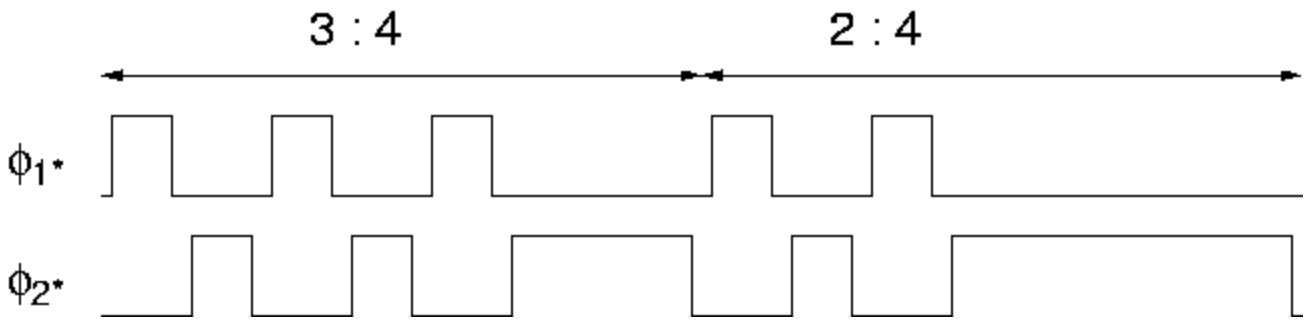

Gnuplot
"biq.data" us 1:2
"biq.data" us 1:3
5
0
-5
-10
-15
-20
-25
-30
-35
-40
1e+07

```
title: biquad (Fleischer,Laker F-type)
/* == fs = 60MHz or 60MHz/15MHz,
fo = 10MHz == */
  timing;
   period 1.667e-08;
   clock clk 1  (0 4/8);
   clock clkQ 4 (0 4/8);
   clock rq   1/100 (0 4/8)
 end;

 /* fully diff. forward int. F1 */
 subckt (1p  4p ) F1 (K:clk P:cap);

   s1p (1p 2p) clk;
   s2p (2p 0) #clk;
   s3p (3p 0) #clk;
   s4p (3p 4p) clk;

   Cp  (2p 3p) cap;
 end;

 /* model for op amp */
 subckt (1 2 3 4) opamp (P:a0);
/* gain is 570, BW = 693e3 */
            E1  (5 0 3 4) 1;
            E2  (1 2 8 0) 570.4;
            S1a (5 6)  rq;
            S1b (8 6) #rq;
            S2a (8 7)  rq;
            S2b (5 7) #rq;
            Ceq (6 7)  28.9e-6;
            Cp  (8 0)  1;
 end;
```

```
/* fully diff. backward int. B1 */
 subckt (1p  4p ) B1 (K:clk P:cap);

   s1p (1p 2p) clk;
   s2p (2p 0) #clk;
   s3p (3p 0) clk;
   s4p (3p 4p) #clk;
     Cp  (2p 3p) cap;
 end;

 /*  ideal integrator with feedback capacitor  */
  subckt (1 2)  ActCap  (P:cap);
   E1 (2 0 0 1) 1e6;
   CF (1 2)  cap;
  end;

/* first biquad in the bp6 filter */
  /* in1 in2 out1 out2 */
  subckt (1 4 12 11 22) biq1 (P:cin P:c1  P:cr
P:cth K:clkSlow);

  /* first OTA */

      X1a (1 4) B1 (#clk cin);
      X1 (22 4) F1 (clk cth);
      X2 (4 11) ActCap (c1);
      X1b (4 11) F1 (clkSlow cr);  /* controls Q */

     /* second OTA  */
     Eneg (11n 0 0 11) 1;
     X3 (11n 12) F1 (#clk cth);
     X4 (12 22) ActCap (c1);


  end;
```

```
circuit;
V1 (1 0);

Xb (1 111 112 113 114) biq1 (1 32 4 32
clkQ);
/* without subsampling */
Xbb (1 1111 1112 1113 1114) biq1 (1 32 4
32 clk);

end;

analyze sss;
set V1 ac 1.0 0.0;
infreq 1e6 30e6 log 100;
print vdb(113) vdb(1113);
end;
```

Time-varying masking signals can be used to fine-tune programming parameters at the cost of increased complexity in digital circuits.



The technique is quite successful for high sampling rate ratios. For low sampling ratios, as required for high speed filters, precautions must be taken to deal with aliasing problems.

Advantages of periodical nonuniform individual sampling:

- •Transfers complexity in the design from analog to digital section,
- • Reduces capacitance spread, hence relaxes the specifications for the OTAs,
- • Introduces an additional degree of freedom in the design.

Periodic Non-Uniform Switched-Capacitor Remarks

Advantages:

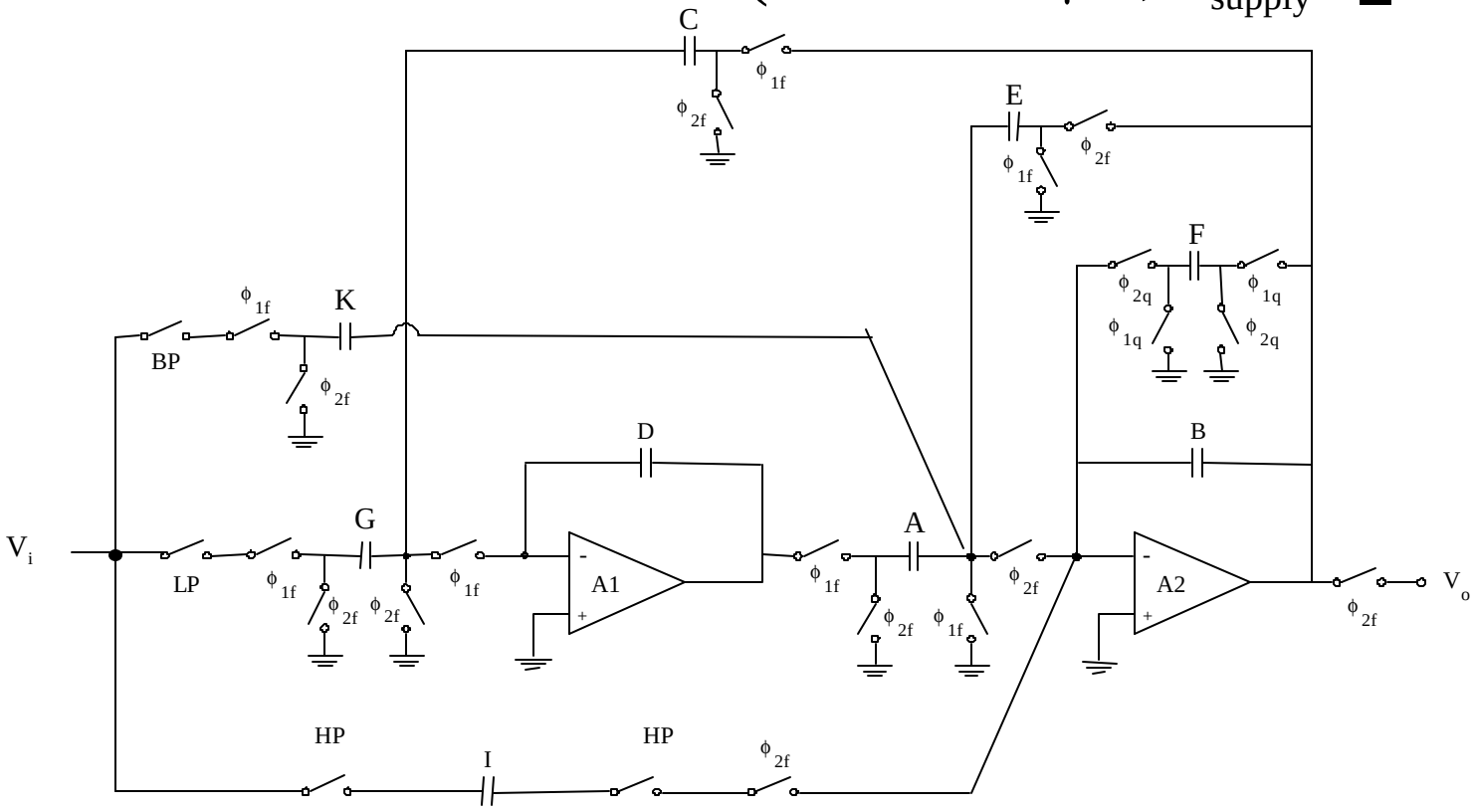
- Great flexibility and resolution for programming SC signal processors.
- The design is performed in the digital domain with a single logic programmable section (i.e., FPGA).
- Reduced cost (area) and high accuracy (no extra parasitic capacitances) respect to any other programming technique (i.e., capacitor arrays).
- Only one clock is used. One sub-clock (ϕ_i) is required for each output response parameter to be programmed.
- The programmability does not affect the circuit dynamic range.

Disadvantages:

- The master clock frequency must be *m* times the clock frequency of the traditional case (p_i=*m*). However, the amplifier requirements remain unchanged.

Example of the Proposed Technique

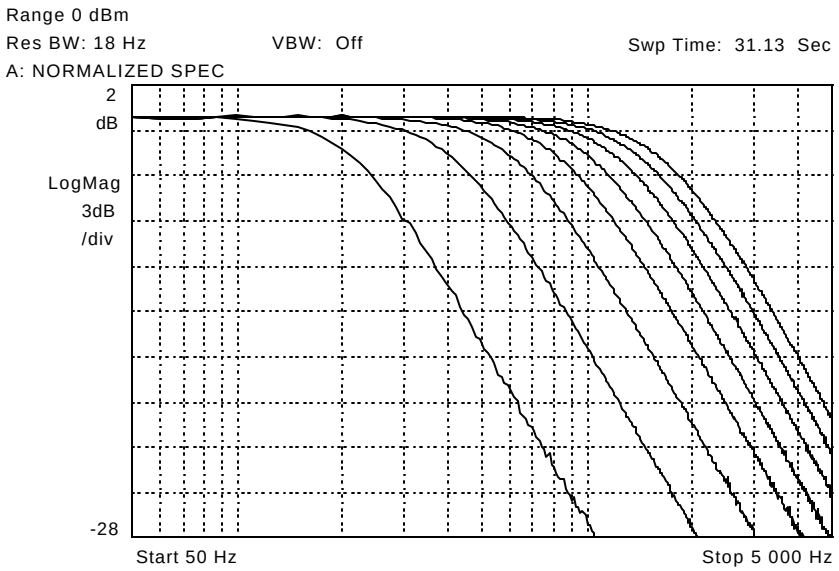
•Universal second-order SC filter (CMOS 1.2 μm, $V_{supply} = \pm 1.5$ V)



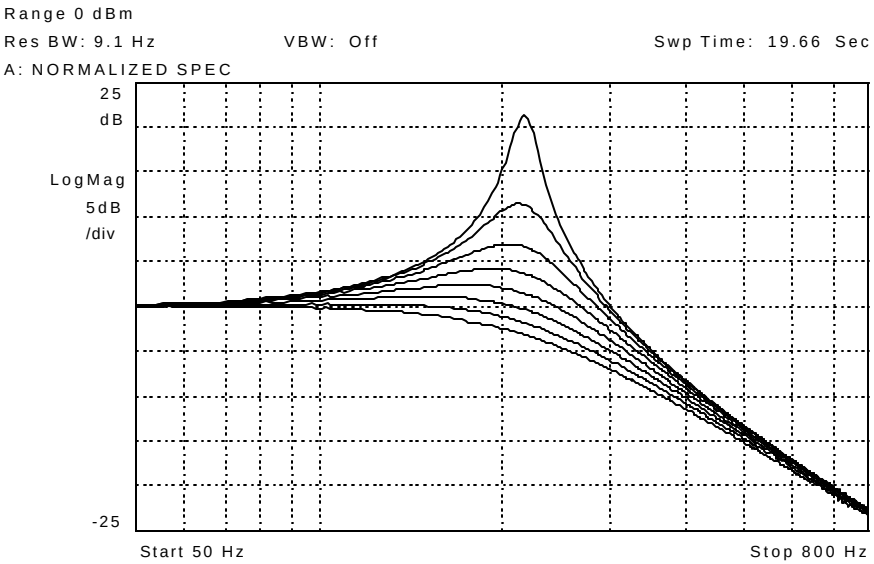
- Design specifications { f_o = 0.2 kHz, Q = 0.707, k = 0 dB } with f_s = 20 kHz
- The SC circuit was designed to operate with clock frequencies up to 1 MHz
- The digital programming signals were off-chip generated by a commercial FPGA

Experimental Results of Second-Order Non-Uniform SC

1. **Low-pass** response programmability (m = 8, f_s = 160 kHz)



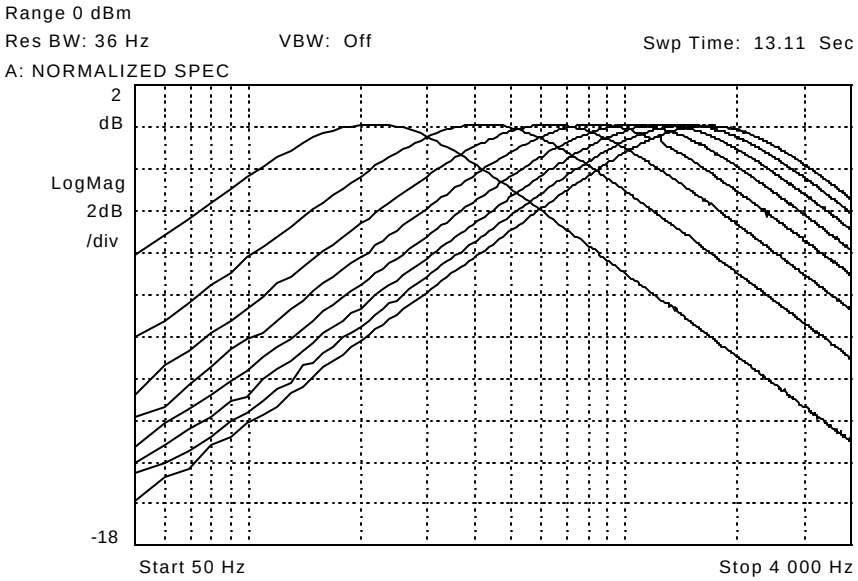
LP f_o-programmability
($1 \leq p_f \leq 8$)



LP Q-factor programmability
($1 \leq p_q \leq 8$)

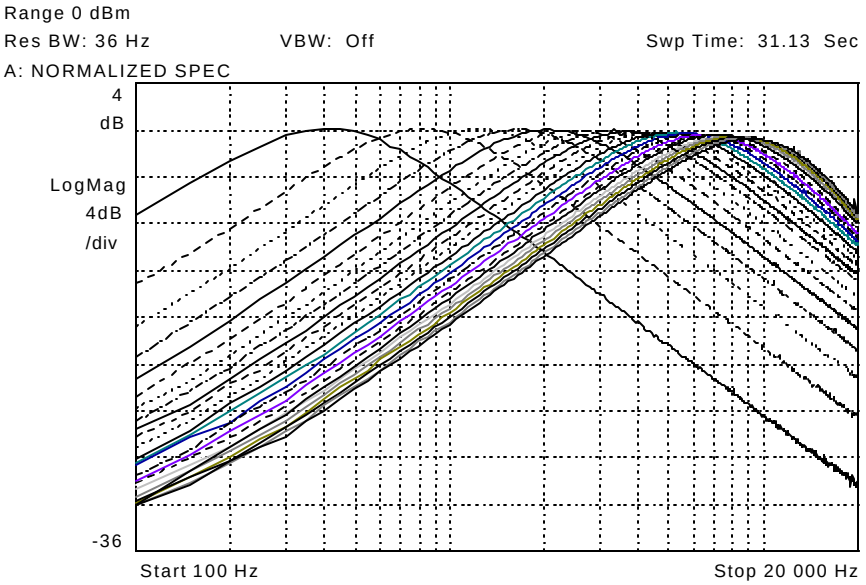
Experimental Results (continues)

2. f_o **Band-pass** response programmability



$m = 8$; $f_s = 160$ kHz

$(1 \leq p_f \leq 8)$



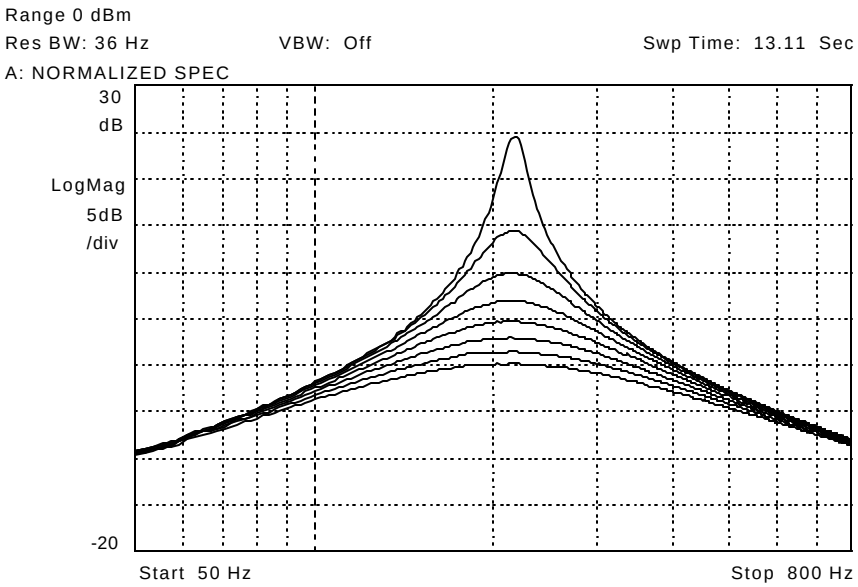
$m = 24$; $f_s = 960$ kHz

$(1 \leq p_f \leq 24)$

Note the increased resolution

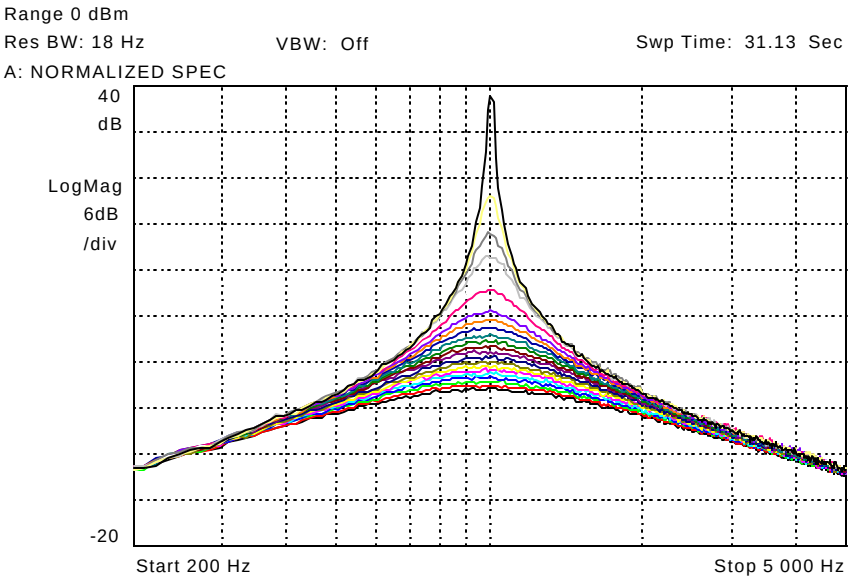
Experimental Results (continues)

3. *Q*-factor band-pass programmability



$m = 8$; $f_s = 160$ kHz

$(1 \leq p_q \leq 8)$



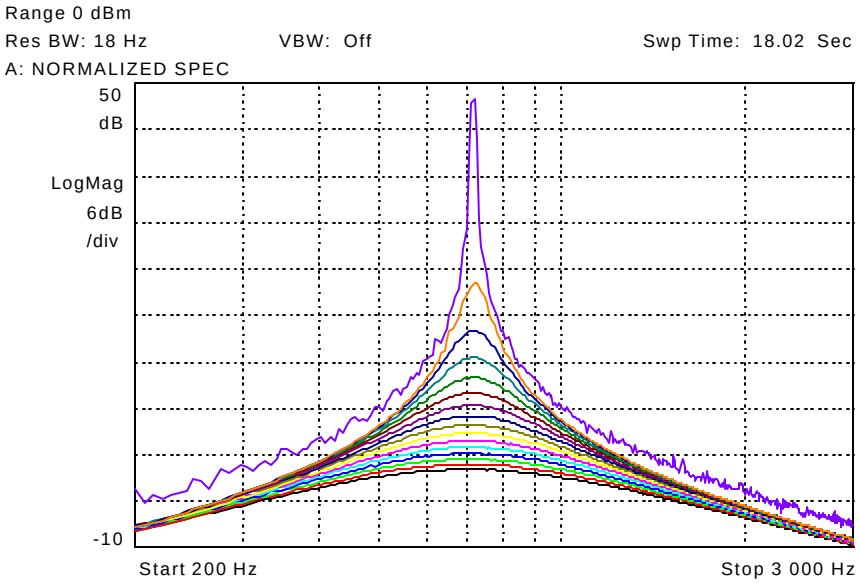
$m = 32$; $p_f = 3$; $f_s = 1$ MHz

$(1 \leq p_q \leq 25)$

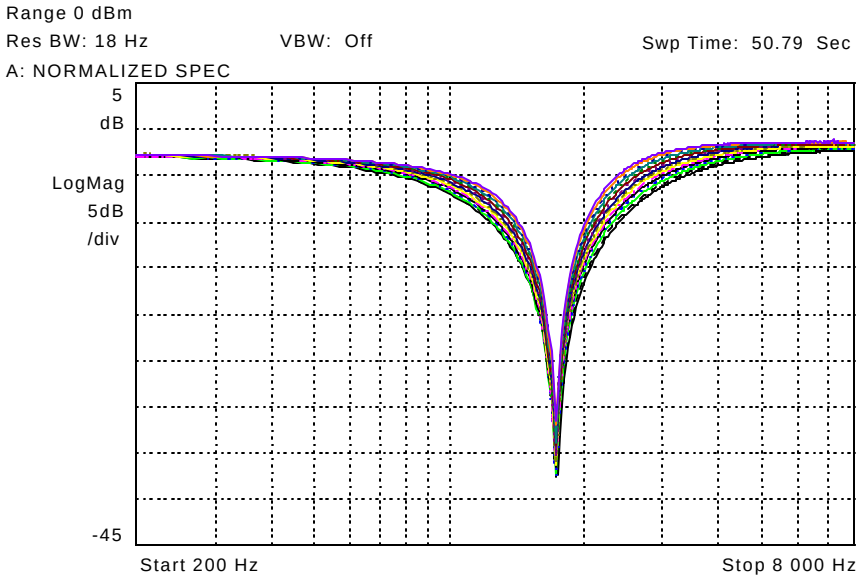
Enhanced Resolution

Experimental Results (continues)

4. *Q*-factor **Band-pass and Notch** programmability

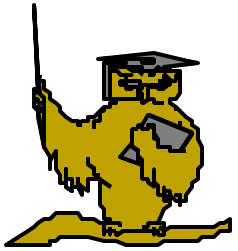


$m = 32$; $p_f = 2$; $f_s = 0.8$ MHz
$(1 \leq p_q \leq 16)$



$m = 24$; $f_s = 1$ MHz
$(1 \leq p_q \leq 16)$

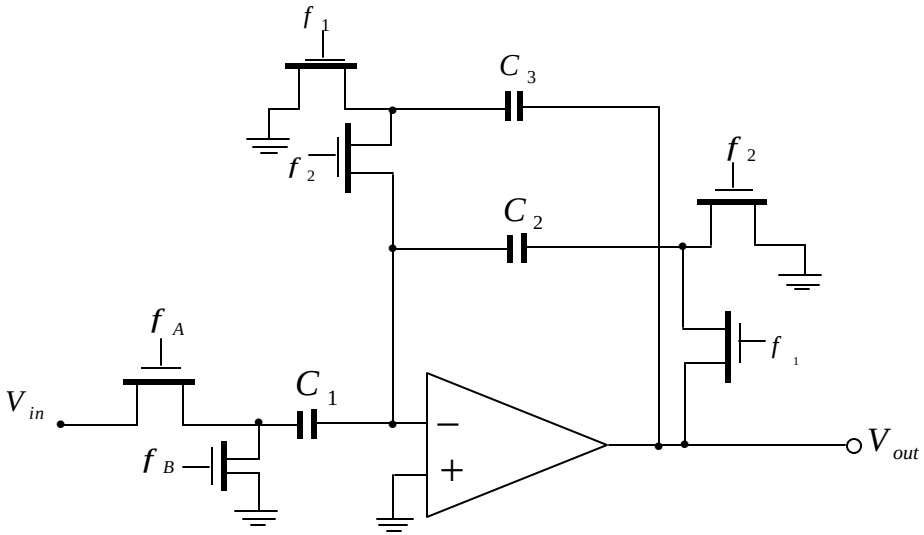
Conclusions



A SC technique with an additional degree of freedom is presented.

Potential applications are very wide and practical implications are very promising.

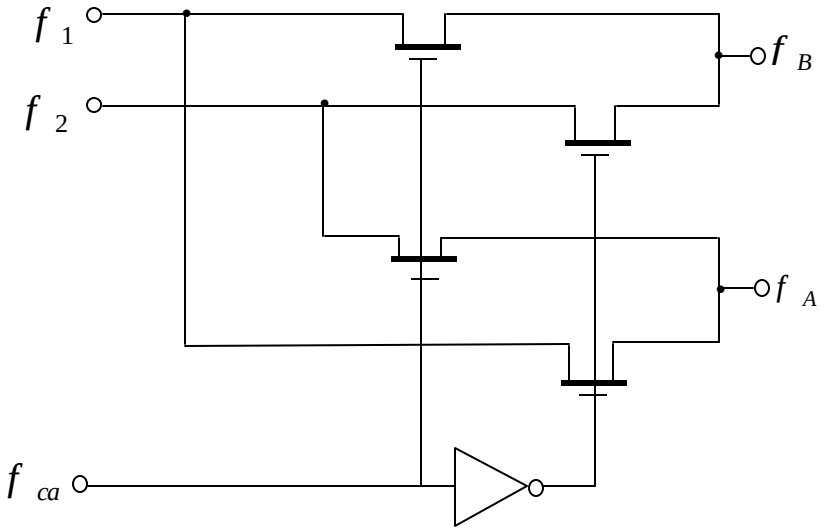
The ideal situation of analog processing and digital control are present in the proposed scheme.



$$f_A = (f_2 \bullet f_{ca}) + (f_1 \bullet \bar{f}_{ca})$$

$$f_B = (f_1 \bullet f_{ca}) + (f_2 \bullet \bar{f}_{ca})$$

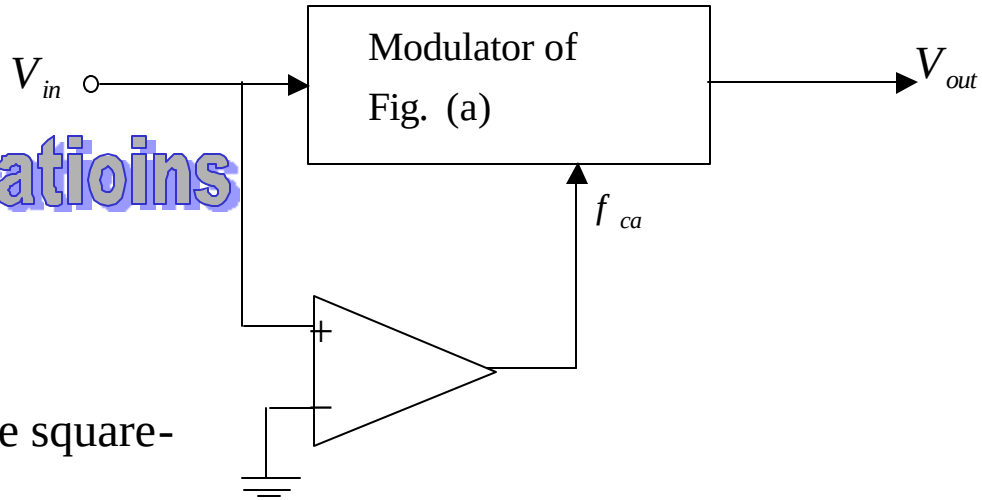
(a)



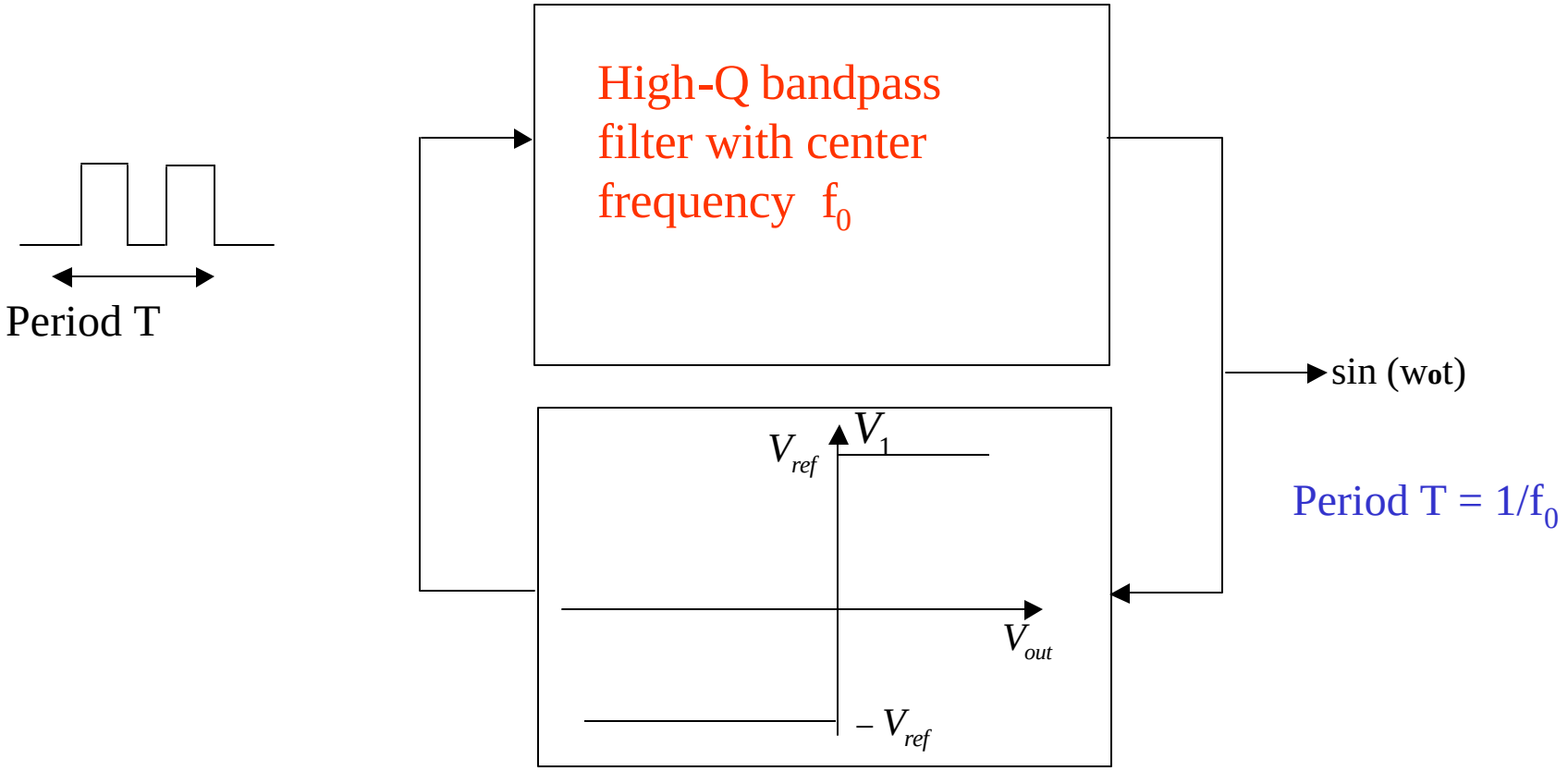
(b)

(a) A switched-capacitor square-wave modulator where the input clock phases are controlled by the modulating square wave ϕ_M. (b) A possible circuit realization for ϕ_A and ϕ_B.

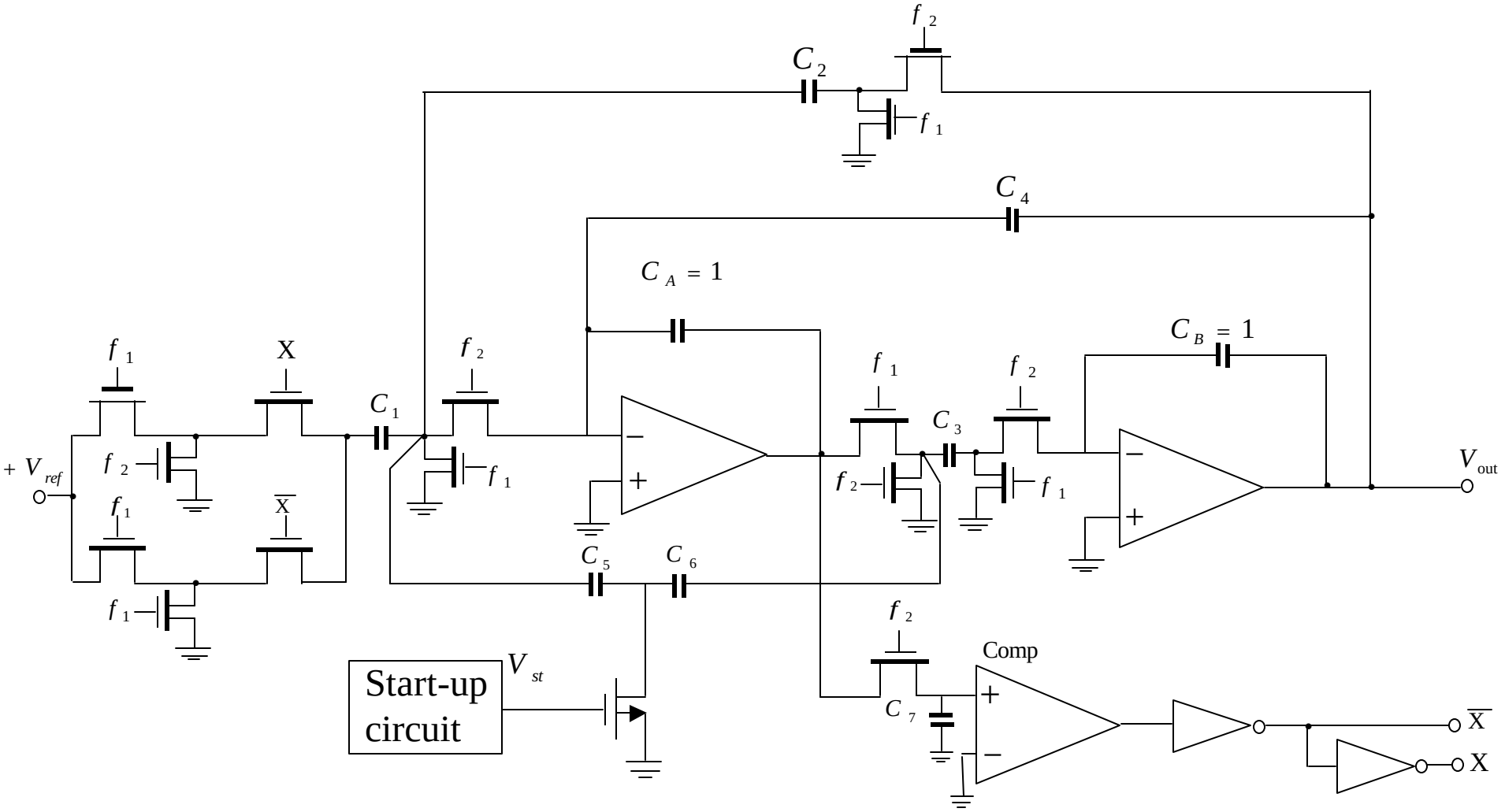
Non-Linear SC Applicatioins



A full-wave detector based on the square-modulator circuit of Fig. (a)



A BP Filter based sinusoidal oscillator.



A SC implementation of a BP based Oscillator

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- E. Sánchez-Sinencio, J. Silva-Martínez, and R.L. Geiger, "Biquadratic SC Filters with Small GB Effects," *IEEE Trans. Circuits and Systems*, Vol. CAS-31, No. 10, pp.876-884, October 1984.

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J. Adut and J. Silva-Martínez, “A high-Q switched-capacitor filter with reduced capacitance spread using a randomized noninterval sampling technique”, ISCAS 2002 submitted.