Midterm Exam 1

EEE598D Analog Filter & Signal Processing Circuits

Spring 2002
Arizona State University

Instructor: Dr. Hongjiang Song

Exam Time: 7:40am – 8:55am Tuesday, February 26, 2002

Name: Solution

ID#: _____

General instruction: This is a closed book/notes exam. However, you may bring a piece of paper (81/2x11) with useful notes. You may also bring a calculator to exam.

All MOS transistors in this exam are assumed to be ideal. That is, the current can be expressed by

$I_d = \beta (V_{gs} - V_T - V_{ds}/2)V_{ds}$ in linear operation mode, or

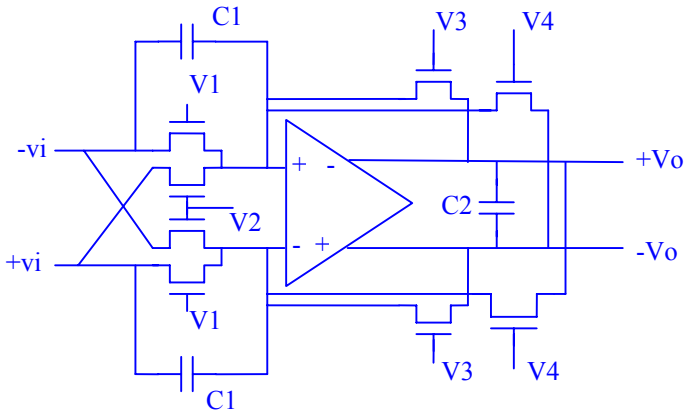
$I_d = \frac{\beta}{2}(V_{gs} - V_T)^2$ in saturation operation mode.

You may also ignore body effect of the device.

Good luck!

ID#: _____ **Solution**

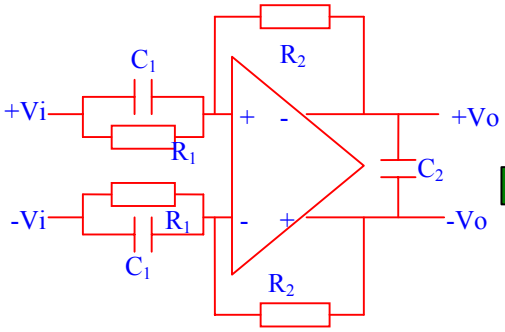
Problem 1. A fully differential MOS-C filter using 4-transistor MOS resistor is shown in Fig.1. All MOS transistors shown are identical and in linear operation mode. Assuming 0v common-mode voltage at all nodes, and an ideal Opamp.

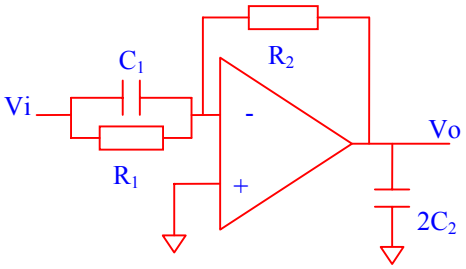


$C_1 = 2C_2 = C$
$V_1 - V_2 = Vx > 0$
$V_3 - V_4 = (1/10)\,Vx$

Fig.1 Fully differential MOS-C filter

a) Draw the single-end active RC equivalent circuit of the filter (5 points)





Where

$$R_1 = \frac{1}{\beta(V_1 - V_2)} = \frac{1}{\beta V_x}$$

$$R_2 = \frac{1}{\beta(V_3 - V_4)} = \frac{10}{\beta V_x}$$

b) Derive the s-domain transfer function of the filter in term of β, V_x, and C (5 points)

$$\frac{V_O(s)}{V_i(s)} = -\frac{R_2}{R_1 // (\frac{1}{sC_1})} = -\frac{(\frac{10}{\beta V_x})}{(\frac{1}{\beta V_x}) // (\frac{1}{sC})} = -\frac{\beta V_x + sC}{\frac{\beta V_x}{10}}$$

or

$$H(s) = \frac{V_o(s)}{V_i(s)} = -10\frac{\frac{\beta Vx}{C} + s}{\frac{\beta Vx}{C}}$$

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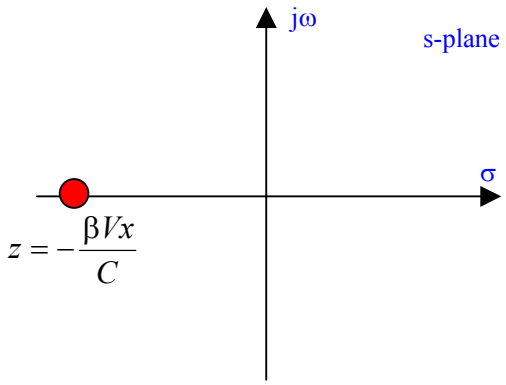
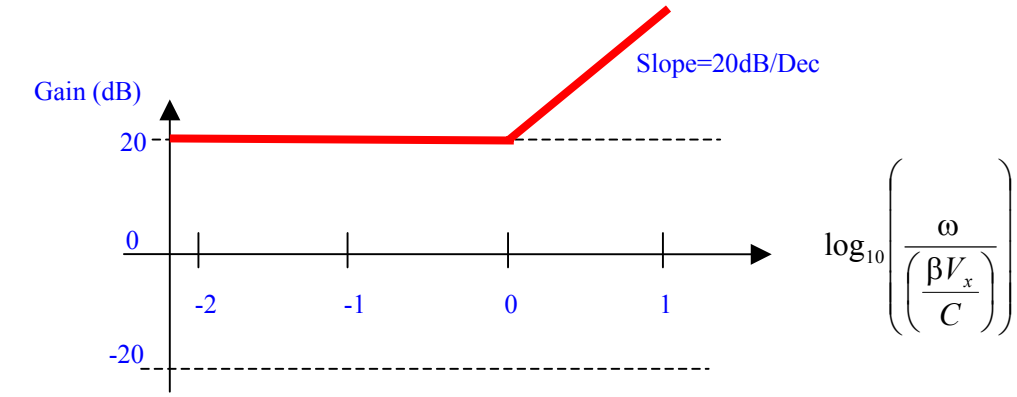
c) Plot the zero and pole of the transfer function in the s-plane (5 points)

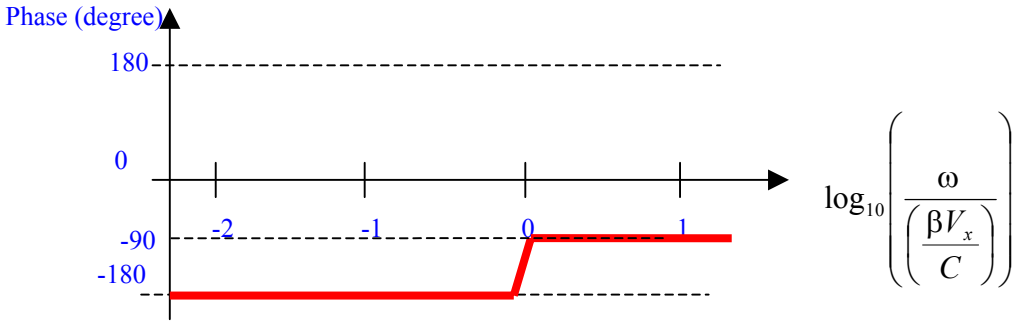


No finite pole

one zero at $z = -\frac{\beta Vx}{C}$

d) Sketch the gain and phase responses of the filter (10 points)





ID#: _____ **Solution**

Problem 2. An inverter-based Gm-C filter circuit is shown in Fig. 2a. Assume that all MOS transistors are in saturation mode. To simplify the problem, we further assume that all NMOS and PMOS transistors are identical respectively, and that $\beta n = \beta p = \beta$, $V_{Tn} = |V_{Tp}| = V_T$.

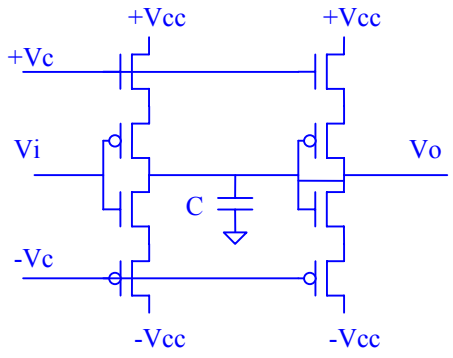


Fig.2a Gm-C filter circuit

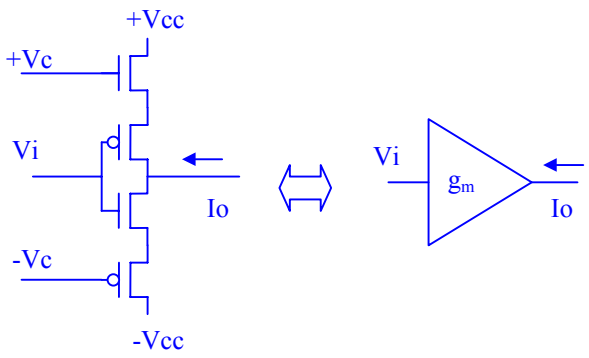


Fig.2b Basic Gm cell

a) Express the transconductance g_m of the basic Gm cell in term of β, V_T and V_C (5 points)

For CMOS pair shown in Fig.2c, we have

$$I_n = \frac{\beta_n}{2}(V_n - V_x - V_{Tn})^2 = I \quad and \quad I_p = \frac{\beta_p}{2}(V_x - V_p - |V_{Tp}|)^2 = I$$

$$\Rightarrow \sqrt{I_n} + \sqrt{I_p} = \sqrt{\frac{\beta_n}{2}}(V_n - V_x - V_{Tn}) + \sqrt{\frac{\beta_p}{2}}(V_x - V_p - |V_{Tp}|)$$

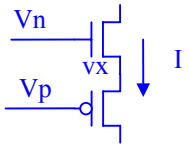


Fig.2c

The above equation can be further simplified using given conditions:

$$2\sqrt{I} = \sqrt{\frac{\beta}{2}}(V_n - V_x - V_T) + \sqrt{\frac{\beta}{2}}(V_x - V_p - V_T) = \sqrt{\frac{\beta}{2}}(V_n - V_p - 2V_T) \Rightarrow I = \frac{\beta}{8}(V_n - V_p - 2V_T)^2$$

Use the above equation to calculate the gm yields:

$$I_o = \frac{\beta}{8}(V_i - (-V)_c - 2V_T)^2 - \frac{\beta}{8}(V_c - V_i - 2V_T)^2$$

$$= \frac{\beta}{8}[(V_i - (-V)_c - 2V_T) + (V_c - V_i - 2V_T)][(V_i - (-V)_c - 2V_T) - (V_c - V_i - 2V_T)]$$

$$= \frac{\beta}{8}[2V_c - 4V_T][2V_i] = \frac{\beta}{2}[V_c - 2V_T][V_i] \Rightarrow \boxed{g_m = \frac{I_o}{V_i} = \frac{\beta}{2}[V_c - 2V_T]}$$

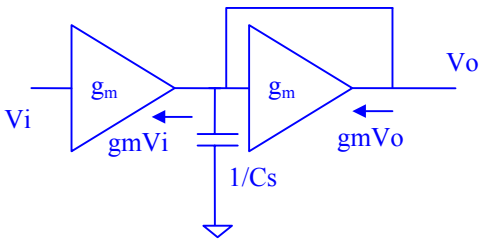
b) Derive the s-domain transfer function of the filter in term of g_m, and C. (5 points)

At node Vo:

$$\sum I = 0 \Rightarrow g_m V(s)_i + g_m V_o(s) + V_o(s)/(\frac{1}{sC}) = 0$$

$$\Rightarrow (g_m + sC)V_o(s) = -g_m V_i(s)$$

$$\Rightarrow \boxed{H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{g_m}{g_m + sC} = -\frac{g_m / C}{g_m / C + s}}$$



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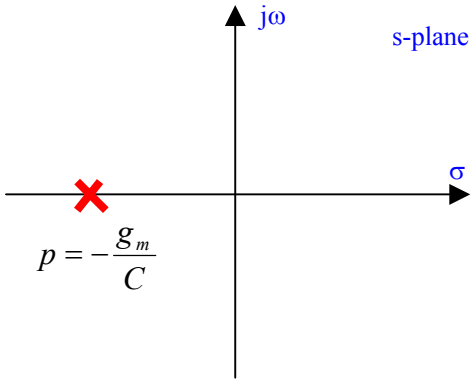
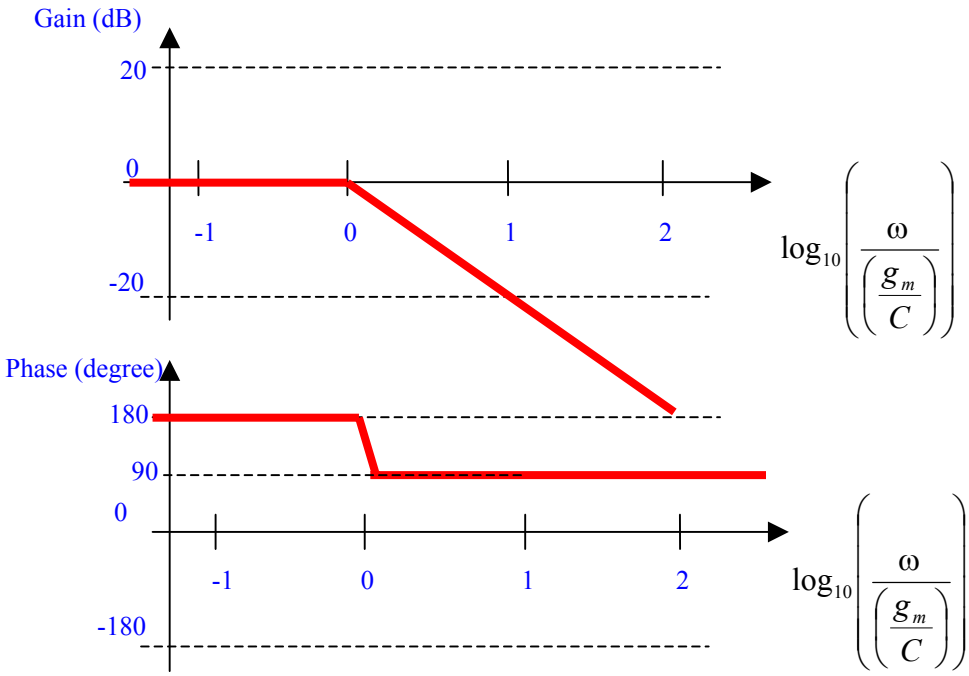
c) Plot the pole and zero of filter transfer function in the s-plane (5 points).



One pole at $p = -\frac{g_m}{C}$

No finite zero

d) Sketch the gain and phase responses of the filter (10 points)



ID#: _____ **Solution**

Problem 3. The following are questions of some basic analog filter concepts covered in the courses. Please **circle** the correct (or the best) answer to the given question (only **ONE** selection per question!). Please remember, since your time is tight, so **don't spend too much time on each question**. It is OK to guess the answer if you are not sure the correct answer to certain question.

3.1) (5 point) In the SI circuit shown in Fig.3.1, device M1 is usually added for the purpose of

a) Gain error minimization
b) CFT (or charge injection) minimization
c) Channel length modulation minimization
d) Device mismatch minimization

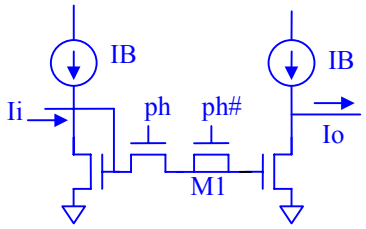


Fig. 3.1

3.2) (5 points) Select the transfer function which corresponding to the SC circuit shown in Fig.3.2.

a) $H(z) = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$ b) $H(z) = -\frac{C_2}{C_1}\frac{z^{-1}}{1-z^{-1}}$

c) $H(z) = +\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$ d) $H(z) = +\frac{C_2}{C_1}\frac{z^{-1}}{1-z^{-1}}$

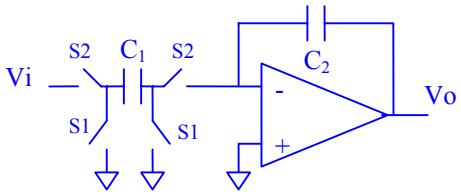


Fig. 3.2

3.3) (5 points) Select the transfer function which corresponding to the SC circuit shown in Fig.3.3.

a) $H(z) = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$ b) $H(z) = -\frac{C_2}{C_1}\frac{z^{-1}}{1-z^{-1}}$

c) $H(z) = +\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}$ d) $H(z) = +\frac{C_2}{C_1}\frac{z^{-1}}{1-z^{-1}}$

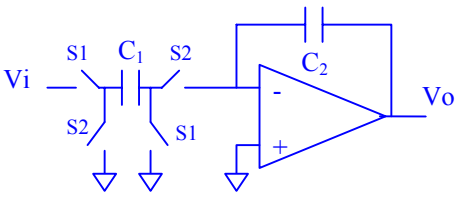
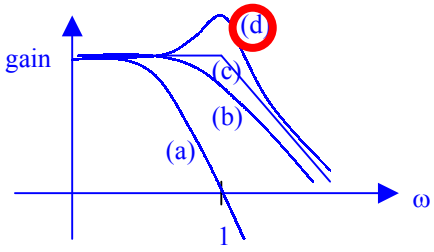


Fig. 3.3

3.4) (5 points) The pole and zero plots of a filter is shown in Fig.3.4. Select a gain response from 4 gain responses below which best describes this filter.



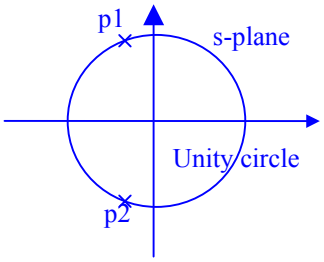


Fig. 3.4

3.5) (5 points) The SFG of a CT filter is shown in Fig. 3.5. Select the correct transfer function for this filter.

a) $H(s) = \frac{s}{s^2+s+1}$ b) $H(s) = \frac{s}{s^3+s^2+1}$

c) $H(s) = \frac{s}{s^3-s^2-1}$ d) $H(s) = \frac{s^2}{-s^3+s^2-1}$

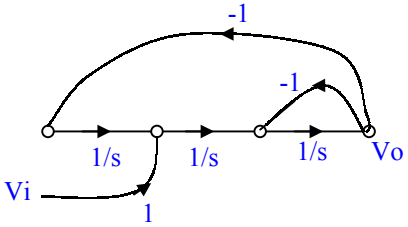


Fig. 3.5

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3.6) (5 points) The major improvement of the 2nd generation (or dynamic) SI circuits (shown in Fig. 3.6) vs. the 1st generation SI circuits is:

a) Better drive capability
b) Better linearity
c) Better device matching
d) Better stability

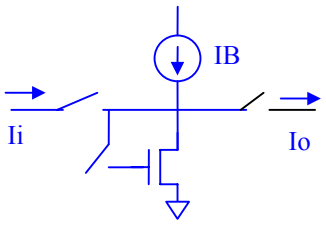

Fig. 3.6

3.7) (5 points) Both SC circuits in Fig.7a and Fig.7b may be used for sample/hold purpose. However, compared with circuit in Fig.7a, the circuit in Fig.7b has the advantage of

a) Better drive capability
b) Smaller Offset error
c) Better device mismatch
d) Smaller layout area

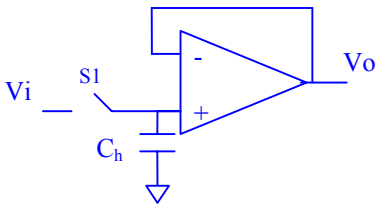

Fig. 3.7a

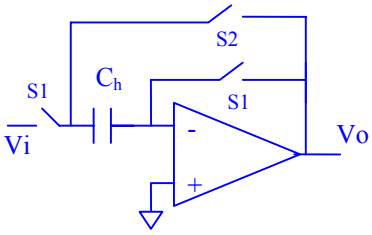

Fig. 3.7b

3.8) (5 points) Fig.3.8a vs. Fig.3.8b shown are two possible implementations of SC integrator. However Fig.3.8a is usually used in practical design because of

a) It is smaller
b) It is faster
c) It is more accurate
d) It is more stable

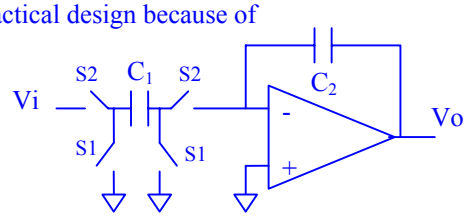

Fig. 3.8a

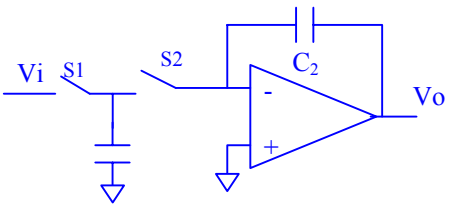

Fig. 3.8b

3.9) (5 points) In SI circuit shown in Fig3.9, device M1 is usually added to

a) Improve circuit stability
b) Reduce the power dissipation
c) Minimize layout area
d) Improve output resistance

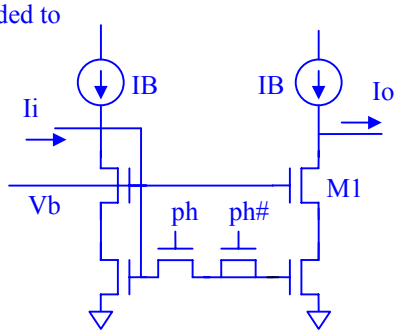

Fig. 3.9

3.10) (5 points) A conventional OTA (operational transconductance amplifier) is not suitable for Gm-C filter design because of its limitation in?

a) Power dissipation
b) Operation speed
c) Linear input operation range
d) Layout area