Subject: Homework #2
Course: EEE598D: Analog Filter & Signal Processing Circuits
Due Date: February 5, 2002 (at the end of class)
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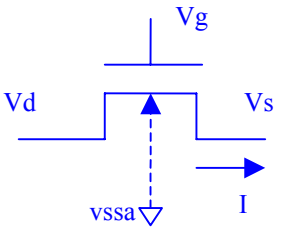
A CMOS mixer topology for use in highly integrated down-converter receiver is shown in Fig.2. An advantage of such architecture is that high frequency (~Ghz) signals can be processed while a low bandwidth (~10Mhz) Opamp is required.
Assuming all transistors shown in the mixer are identical and are operated in triode (or linear region), that is, the current I is given as



$$I = \beta(V_{gs} - V_T - \frac{V_{ds}}{2})(V_d - V_s)$$

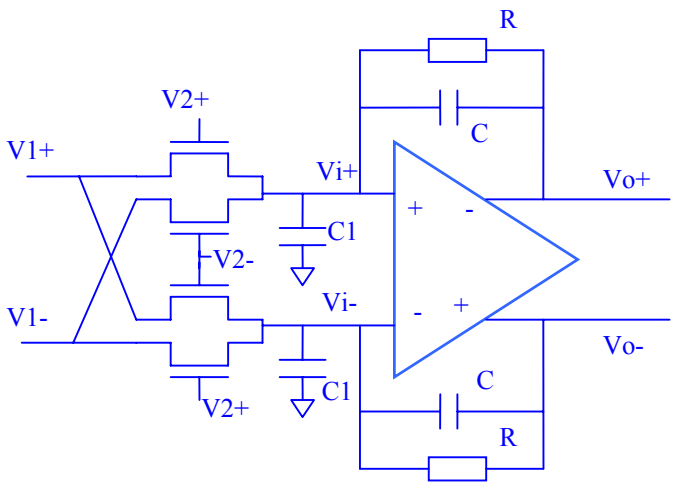


Fig.2 CMOS down-converter mixer structure

Problem 1. Ideal Opamp

a) Derive the s-domain transfer function of the above mixer for an ideal opamp (you may also ignore C1, and assume a 0v common-mode voltage at all points in this case) for given β and V_T:

$$\frac{V_{o+}-V_{o-}}{V_{1+}-V_{1-}}\Big|_{(V_{2+}-V_{2-})=const.}=?$$

$$\frac{V_{o+}-V_{o-}}{V_{2+}-V_{2-}}\Big|_{(V_{1+}-V_{1-})=const.}=?$$

b) Plot the pole and zero in the s-plane.

c) Sketch the Bode Plots.

d) Draw a SFG for this mixer.

Problem 2. Non-ideal Opamp

For a given single-pole opamp with DC gain Ao and bandwidth ωo:

$$\frac{V_{o+}-V_{o-}}{V_{in+}-V_{in-}}=\frac{A_o}{1+s/\omega_o}$$

and include C1.

Hint: you may assume vi+ and vi- are very close to simply the calculation of the 4-T MOS VCR resistance.

Repeat all questions in Problem 1.