ICT ALGORITHM TYPE 2 PROGRAM/VERIFY SPECIFICATION

For PEEL^{TM}18CV8

Revision E, April, 1999

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REVISION HISTORY

REVISION NUMBER	DATE	DESCRIPTION
1.1	08/09/94	Changed Term Group Address for signature.
1.2	08/25/94	Changed Verify and Program waveforms.
2.0	09/27/94	Changed Verify and Program Waveforms
2.1	10/31/99	Revised V_{PP} voltage using 15.5V recommended.
A	12/21/94	Changed V_{HH} from 14.5 - 15.0 to 14.0 - 14.5.
B	12/23/94	Revised Signature Word Address.
C	07/29/96	Complete rewrite of Spec.
D	08/22/99	Changed incorrect table references. Added “W” to Diagram column of AC Electrical Characteristics chart and addes “S” and “W” definitions to AC Electrical Characteristics chart.
E	04/30/99	Complete rewrite of Spec. and recreate all diagrams.

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1.0 INTRODUCTION

This document contains the necessary technical specifications for proper program/verify operations of the PEEL^{TM}18CV8 Programmable Electrically Erasable Logic devices. Information provided assumes the reader has a general knowledge of PLDs and has read the PEEL18CV8 data sheet (August 1986 or later version). It is recommended to use the PEEL18CV8 data sheet in conjunction with this Specification.

2.0 PRE-CONDITIONING

The PEEL^{TM}18CV8 requires a pre-conditioning prior to programming. This pre-conditioning, which ensures better reliability in the PEEL^{TM}18CV8, involves the ERASE ALL and PROGRAM (WRITE) ALL modes.

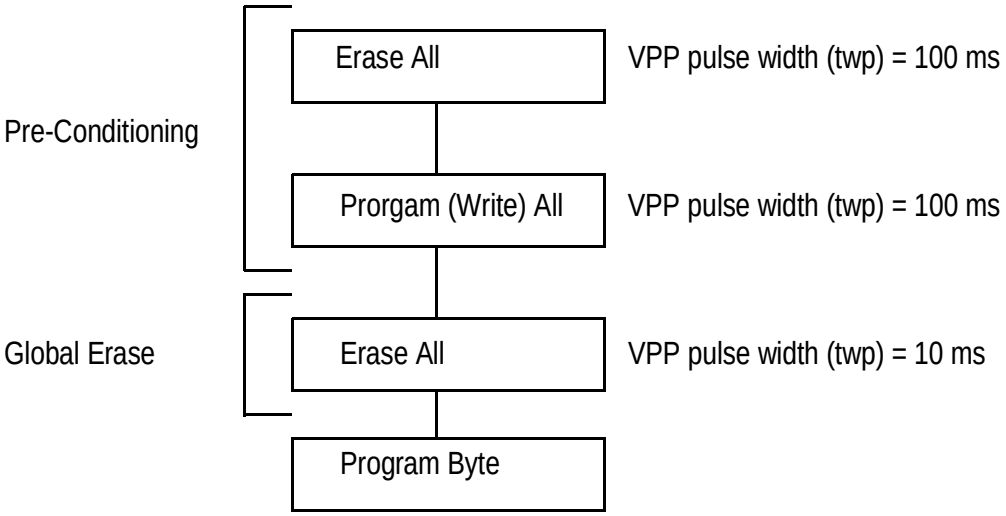

Figure 1 – Pre-conditioning Flowchart

Please note that the only difference between the ERASE ALL mode used for global erasing and preconditioning is the pulse width for the V_{PP} signal. For convenience, all the necessary information such as the AC and DC Electrical Characteristics, Mode Flows and Waveforms are included in this specification.

3.0 PROGRAM/VERIFY OPERATION DESCRIPTION

Program/Verify operation of the PEEL^{TM}18CV8 Programmable Electrically Erasable Logic Device is similar to that of other CMOS PLDs that use a parallel interface scheme. The PEEL^{TM}18CV8 can be enabled for program and verification by raising and holding pin 1 to V_{HH1}. Doing this will cause the pin functions of the PEEL^{TM}18CV8 to change from normal operation to Program/Verify operation as shown in the pin connection diagram and table, Figure 2 and Table 1 respectively. Four of the pins, (PVE, PVP, SEC and ALE/ERA) use high voltage levels to implement specific program/verify functions. All other pins use standard TTL levels with the exception of V_{CC} and GND which must be maintained at +5V and ground respectively.

A total of 2696 programmable electrically erasable cells are used to configure the PEEL^{TM}18CV8. The numbers on the logic array diagram in Figure 3 designate the order each E^2 cell is programmed via the JEDEC "fuse" map. Note that since the PEEL^{TM}18CV8 does not use actual fuses as with bipolar technology, the term fuse is used here purely for the sake of convention. An example JEDEC "fuse" map file is shown in Figure 5.

There are four primary modes used in program/verify operation: Program Byte, Verify Byte, Erase All and Set Security Bit. The selection of these modes are controlled by the Mode A-B pin. Depending on the mode selected, an input line address (IAD_{0-7}) and term group (TGA_{0-3}) must be set to a specific value as listed in Program/Verify Tables 3-6. Besides input addressing, the multiplexed IAD_{0-7} pins are also used for programming fuse state data from the JEDEC fuse map as shown in Table 7.

When reading (verifying) data from the PEEL^{TM}18CV8, a 0 data bit equals a "connected fuse" and a 1 equals an "open fuse" as with the standard JEDEC fuse map convention. However, when writing (programming) data to the PEEL18CV8, the data must first be inverted from that of the JEDEC map for correct program operation. After the PEEL18CV8 is erased, the "fuse states" will all be open. The macrocell after erasure will default to macrocell configuration 1 as specified in Table 2 of the PEEL18CV8 (August 1986 or later) data sheet. This table lists the 12 configurations that each macrocell can be programmed into via A, B, C and D configuration bits.

Demultiplexing of the IAD_{0-7} is accomplished using the ALE/ERA pin in conjunction with the PVP (program/verify pulse) pin. ALE/ERA latches the address when raised in V_{IH}. Before ALE/ERA can be brought back to V_{IL}, the PVP pin must have completed its ramp to V_{HH2} (at a 50µS/V or slower rate, see timing diagrams for further detail). The ALE/ERA pin also serves as an enable for the erase all mode when raised to V_{HH2}. Likewise, the SEC pin when raised to V_{HH2} enables the set security bit mode. Once the security bit is set, verification is not possible until the erase all mode is again implemented.

The PVP pin is the primary gating pulse for any mode of operation. Once all other conditions are set up, PVP is ramped to the V_{HH2} high voltage level at a 50uS/V or greater rise time. If the program byte or erase all modes have been selected, the pulse on PVP must be maintained a V_{HH2} for 10ms. If the security mode has been selected, the pulse on PVP must be maintained at V_{HH2} for 300ms. During verify mode, however, PVP need only be held high for 1uS. Less crucial that the rise time, the fall time of PVP can be 1uS or greater. For a complete understanding of the PEEL^{TM}18CV8 programming signals and their relative timings, please refer to the Program/Verify Parameters and Waveform Timing figures of this specification.

For the convenience of deciphering the PEEL^{TM}18CV8 programming algorithms, the procedural flow for each of the four modes is shown in Tables 8-11. Note that the PEEL^{TM}18CV8 should always be erased first before programming any "fuse state" data. Additionally, it is best to start with all pins in a low (V_{IL}) state and then proceed with the Program/Verify operation.

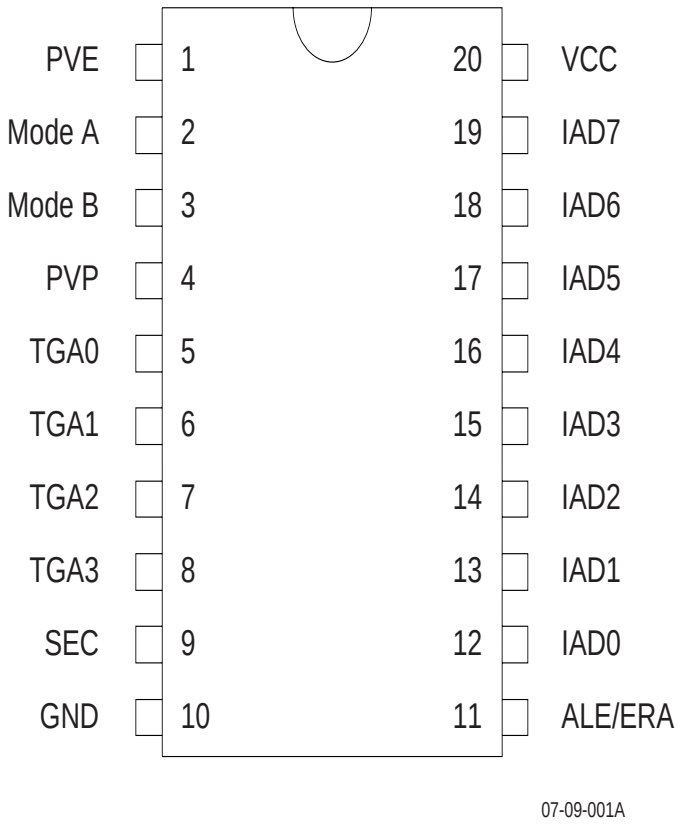

Figure 2⓫ – DIP, SOIC and TSSOP Program/Verify Pin Configuration

Pin Number	Name	Function
1	PVE	Program/Verify Enable
2-3	Mode (A-B)	Erase, Write and Verify Mode Selection
4	PVP	Program/Verify Pulse
5-8	TGA 0-3	Term Group Address
9	SEC/OD	Security Enable
10	GND	Ground
11	ALE/ERA	Input Address Latch/Erase Enable
12-19	IAD 0-7	Input Address/Term Group Data (Fuse State)
20	V_{CC}	Power Supply (+5V)

Table 1[10] – Program/Verify Pin Description

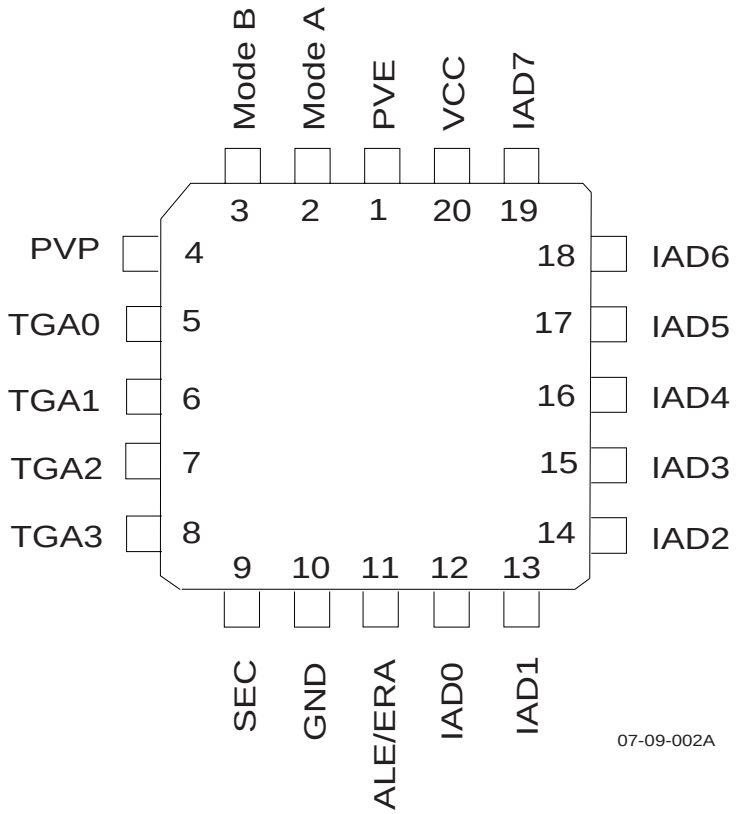

Figure 3– PLCC Program/Verify Pin Configuration

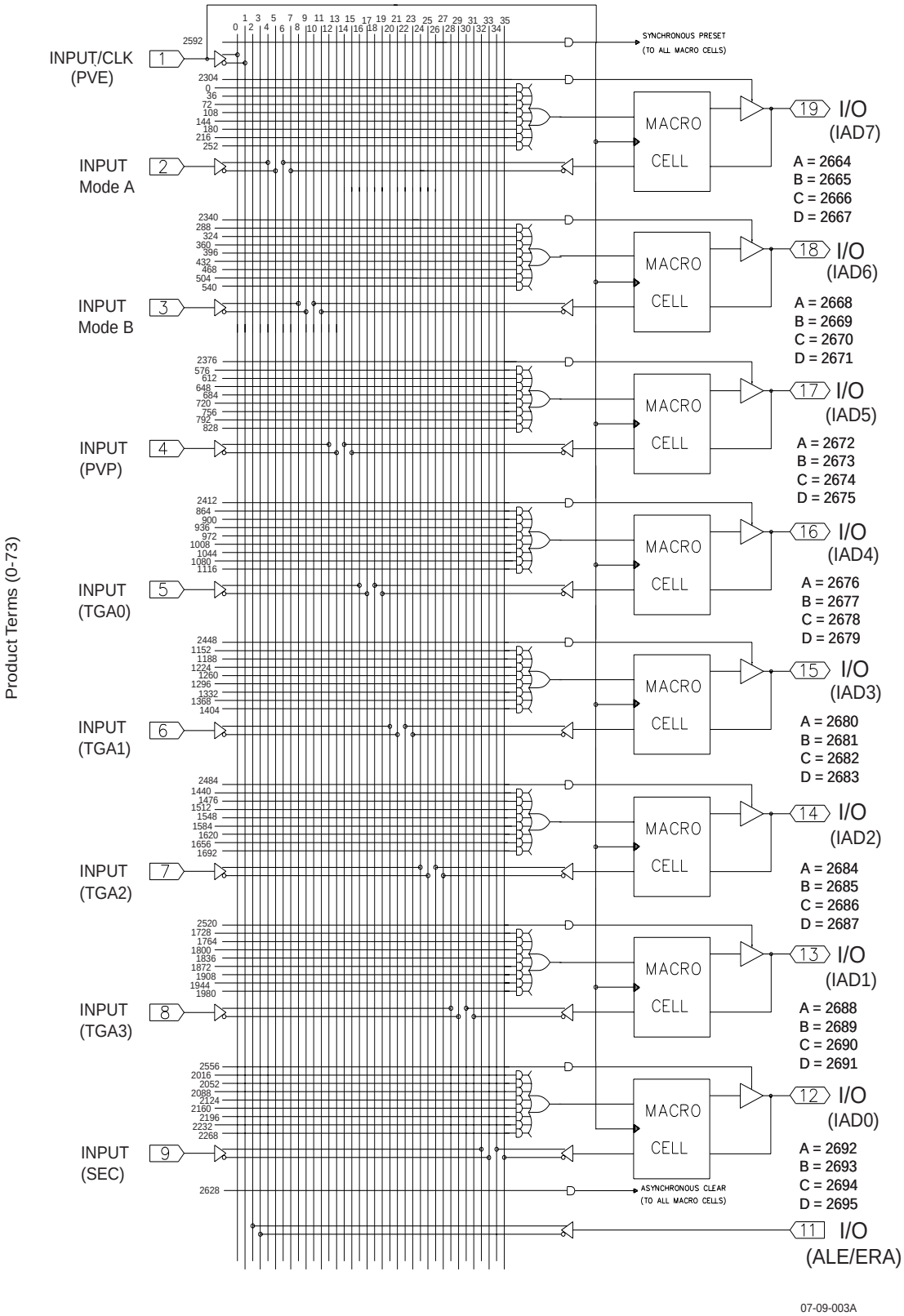

Figure 4[10] – Logic Array Diagram with Fuse Map Numbers

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QF2696

N pin 0011 0011 0011 0011 0011 0011 0011 0011 0011
      1111 2299 3388 4477 5566 6655 7744 8833 9911
      TFTF TFTF TFTF TFTF TFTF TFTF TFTF TFTF TFTF *
N Output Pin 19*
L0000 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0036 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0072 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0108 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0144 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0180 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0216 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0252 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 18*
L0288 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0324 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0360 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0396 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0432 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0468 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0504 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0540 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 17*
L0576 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0612 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0648 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0684 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0720 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0756 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0792 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0828 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 16*
L0864 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0900 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0936 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L0972 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1008 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1044 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1080 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1116 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 15*
L1152 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
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L1188 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1224 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1260 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1296 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1332 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1368 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1404 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 14*
L1440 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1476 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1512 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1548 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1584 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1620 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1656 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1692 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 13*
L1728 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1764 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1800 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1836 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1872 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1908 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1944 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L1980 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Pin 12*
L2016 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2052 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2088 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2124 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2160 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2196 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2232 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2268 0101 0101 0101 0101 0101 0101 0101 0101 0101 *

N Output Enable 19,18,...12*
L2304 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2340 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2376 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2412 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2448 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2484 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2520 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2556 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
```

```
N Sync Preset, Async Clear, Macrocell 19,18,...12*
L2592 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2628 0101 0101 0101 0101 0101 0101 0101 0101 0101 *
L2664 0101 0101 0101 0101 0101 0101 0101 0101 *

CDFCA*
_0000
```

Figure 5 – JEDEC Fuse Map Example

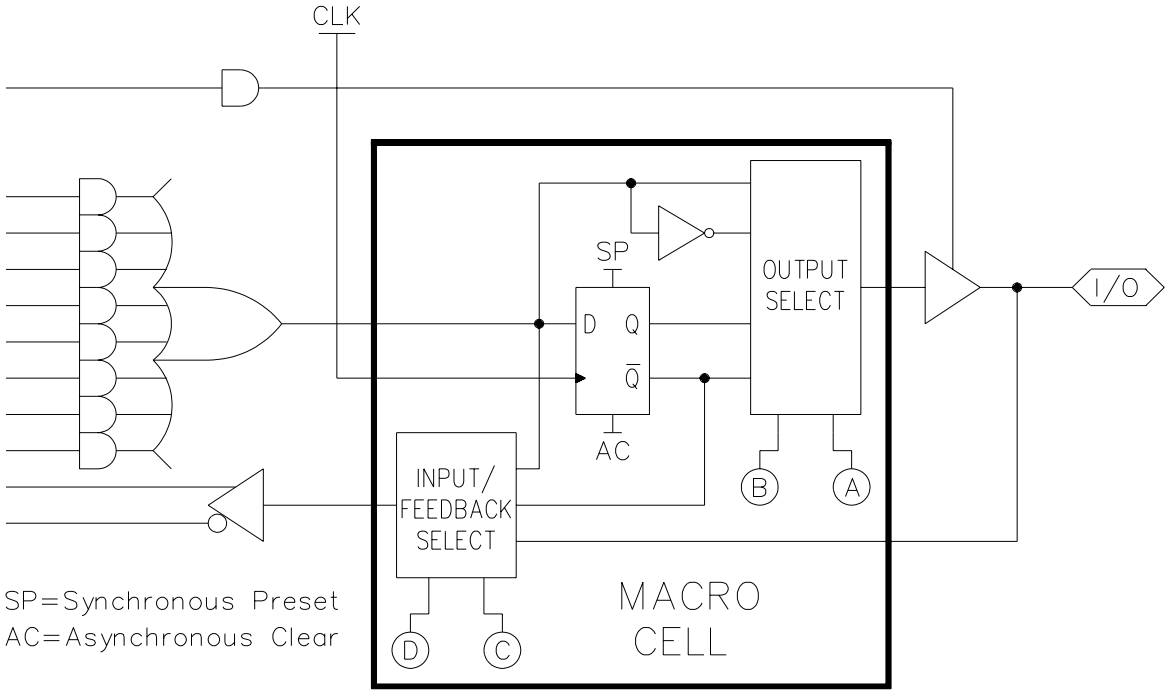

Figure 6 – Macrocell Block Diagram

Configuration					Input/Feedback Selection	Output Selection	
Number	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active Low
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

Table 2 – Macrocell Configuration Bits

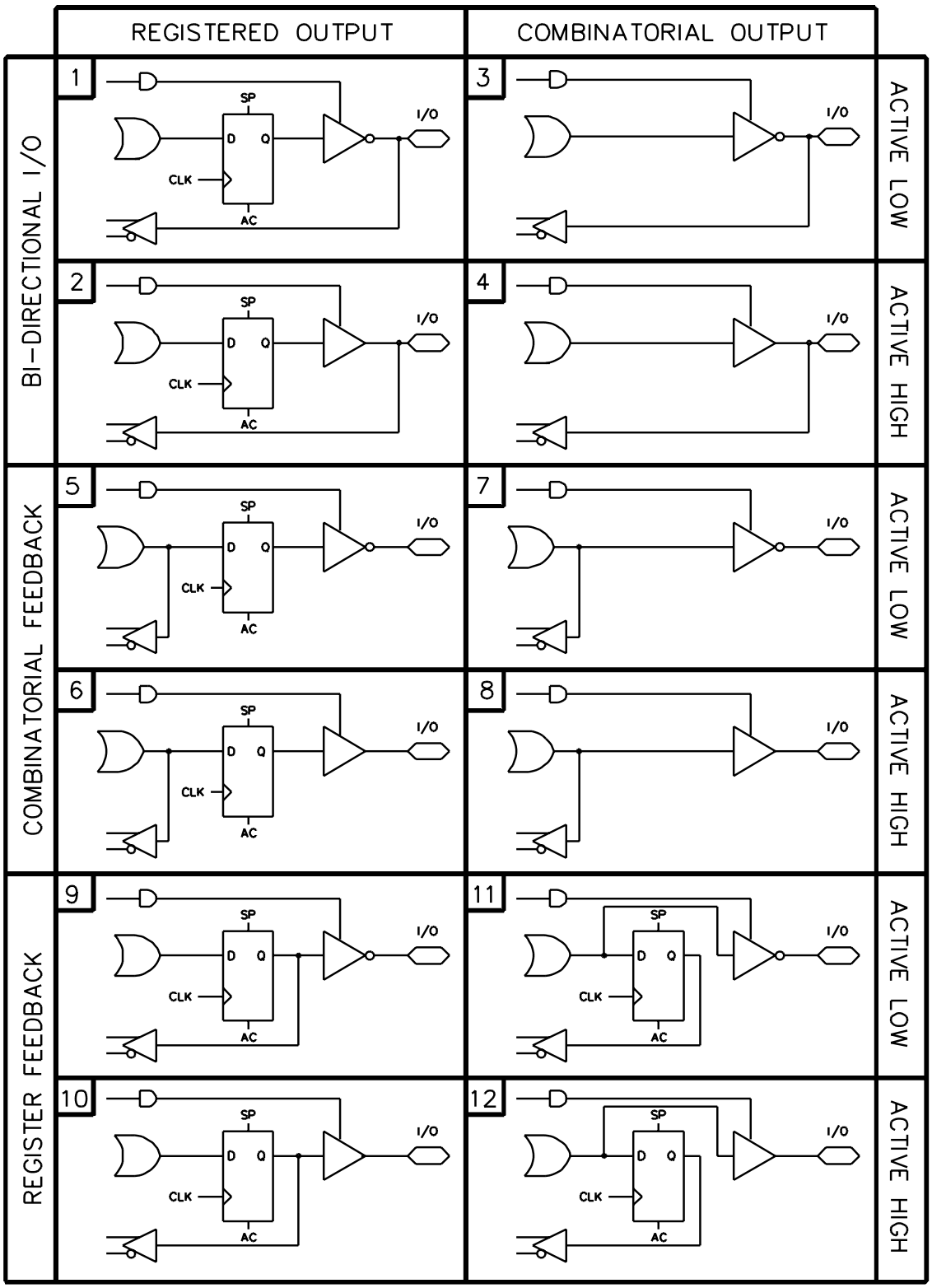

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Figure 7 – Macrocell Configuration Equivalent Circuits

4.0 PROGRAM/VERIFY REFERENCE TABLES

Operation Modes	Program/Verify Pins							
	PVE Pin 1	Mode A Pin 2	Mode B Pin 3	PVP Pin 4	SEC Pin 9	ALE Pin 11	TGA (0-3) Pins 5-8	IAD (0-7) Pins 12-19
Normal Operation	X	X	X	X	X	X	X	X
Erase All	H1	0	0	H2	0	H2	0h	00h
Program Byte	H1	1	1	H2	0	^1	(See Tables 4-7)	
Verify Byte	H1	1	0	H2	0	^1	(See Tables 4-7)	
Set Security Bit	H1	1	1	H2	H2	^1	0h	00h

① The rise time for PVP during Program/Verify and Security Bit is different.
Please see the flowchart individually for detail.

H1 = V_{HH1}

H2 = V_{HH2}

X = V_{IL} or V_{IH} (TTL Don't Care)

0 = V_{IL} (TTL Low)

1 = V_{IH} (TTL High)

^1 = High Level Latch

Table 3① – General Program/Verify Operation

Input Line Number	Input Function	IAD (7-0)								IAD(7-0) (HEX)	ALE 11
		19	18	17	16	15	14	13	12		
0	PIN 1	0	0	0	0	0	0	0	1	01	^1
1	/PIN 1	0	0	0	0	0	0	1	1	03	^1
2	PIN 11	0	0	0	0	0	0	1	0	02	^1
3	/PIN 11	0	0	0	0	0	1	0	0	04	^1
4	PIN 2	0	0	0	0	0	1	0	1	05	^1
5	/PIN2	0	0	0	0	0	1	1	1	07	^1
6	FB 19	0	0	1	0	0	0	0	1	21	^1
7	/FB 19	0	0	1	0	0	0	1	1	23	^1
8	PIN 3	0	0	0	0	1	0	0	1	09	^1
9	/PIN 3	0	0	0	0	1	0	1	1	0B	^1
10	FB 18	0	0	0	1	1	1	0	1	1D	^1
11	/FB 18	0	0	0	1	1	1	1	1	1F	^1
12	PIN 4	0	0	0	0	1	1	0	1	0D	^1
13	/PIN 4	0	0	0	0	1	1	1	1	0F	^1
14	FB 17	0	0	0	1	1	0	0	1	19	^1
15	/FB 17	0	0	0	1	1	0	1	1	1B	^1
16	PIN 5	0	0	0	1	0	0	0	1	11	^1
17	/PIN 5	0	0	0	1	0	0	1	1	13	^1
18	FB 16	0	0	0	1	0	1	0	1	15	^1
19	/FB 16	0	0	0	1	0	1	1	1	17	^1
20	PIN 6	0	0	0	1	0	0	1	0	12	^1
21	/PIN 6	0	0	0	1	0	1	0	0	14	^1
22	FB 15	0	0	0	1	1	0	0	0	18	^1
23	/FB 15	0	0	0	1	0	1	1	0	16	^1
24	PIN 7	0	0	0	0	1	1	1	0	0E	^1
25	/PIN 7	0	0	0	1	0	0	0	0	10	^1
26	FB 14	0	0	0	1	1	1	0	0	1C	^1
27	/FB 14	0	0	0	1	1	0	1	0	1A	^1
28	PIN 8	0	0	0	0	1	0	1	0	0A	^1
29	/PIN 8	0	0	0	0	1	1	0	0	0C	^1
30	FB 13	0	0	1	0	0	0	0	0	20	^1
31	/FB 13	0	0	0	1	1	1	1	0	1E	^1
32	PIN 9	0	0	0	0	0	1	1	0	06	^1
33	/PIN 9	0	0	0	0	1	0	0	0	08	^1
34	FB 12	0	0	1	0	0	1	0	0	24	^1
35	/FB 12	0	0	1	0	0	0	1	0	22	^1

② "FB #" means FeedBack from the Macrocell # (the "#" corresponds to the pin number).

Table 4⑩ – Input Line Addressing

Input Line Number	Function	IAD (7-0)								IAD(7-0) (HEX)	ALE 11
		19	18	17	16	15	14	13	12		
36	MACROCELLS	0	0	1	0	0	1	0	1	25	^1

Table 5⑩ – Macrocell line Addressing

Term Group Number	Function		TGA(3-0)				TGA(3-0) (HEX)
	Inputs (0-35)	Config (36)	8	7	6	5	
0	PRODUCT TERMS 00-07	MACROCELL 19	1	0	0	0	8
1	PRODUCT TERMS 08-15	MACROCELL 18	0	1	1	1	7
2	PRODUCT TERMS 16-23	MACROCELL 17	0	1	1	0	6
3	PRODUCT TERMS 24-31	MACROCELL 16	0	1	0	1	5
4	PRODUCT TERMS 32-39	MACROCELL 15	0	1	0	0	4
5	PRODUCT TERMS 40-47	MACROCELL 14	0	0	1	1	3
6	PRODUCT TERMS 48-55	MACROCELL 13	0	0	1	0	2
7	PRODUCT TERMS 56-63	MACROCELL 12	0	0	0	1	1
8	OE TERMS 64-71	RESERVED	1	0	0	1	9
9	SP & AC TERMS 72-73	RESERVED	1	0	1	0	A

Table 6⑩ – Term Group Addressing

Input Line Number	Term Group Number	Group Function	IAD(7-0) Pins ③							
			19	18	17	16	15	14	13	12
0-35	0-7	PRODUCT TERMS	LSB----------->MSB							
0-35	8	OE TERMS	LSB----------->MSB							
0-35	9	SP & AC TERMS	X	X	X	X	X	X	SP	AC
36	0-7	MACROCELLS	D	X	C	X	B	X	A	X
36	8	RESERVED	R	X	R	X	R	X	R	X
36	9	RESERVED	X	X	X	X	X	X	R	X

③ All data programmed to the IAD(0-7) pins must first be inverted from its state in JEDEC fuse map. Data read (verified) from the IAD(0-7) pins, however, does not require any inversion for correct correspondence to the fuse map values.

MSB = Most Significant Bit
LSB = Least Significant Bit
X = TTL Don't Care
R = Factory reserved

D, C, B and A = Macrocell Configuration Bits

Table 7⑩ – Term Group Data (Fuse State) Format

5.0 PROGRAM/VERIFY FLOW TABLES

Step	Pin Number	Pin Name	Action
0	12-19	IAD(0-7)	Set to high impedance (Hi - Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set Mode A = V_{IH}, Mode B = V_{IH}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA(0-3)	Set next term group address (See Table 6)
5	12-19	IAD(0-7)	Set next input line address (See Table 4-5)
6	11	ALE/ERA	Set to V_{IH} (Latch address)
7	12-19	IAD(0-7)	Set Data “Fuse State” inverted from JEDEC fuse map (See Table 7)
8	4	PVP	Set to V_{HH2}
9	11	ALE/ERA	Set to V_{IL}
10	4	PVP	Hold for t_{WP} then set to V_{IL}
11	---	---	Repeat step 5-10 until all 36 input lines and 1 macrocell line have been programmed
12	---	---	Repeat step 4-11 until all 10 term groups have been programmed
13	12-19	IAD(0-7)	Set to high impedance (Hi - Z)
14	1	PVE	Set to V_{IL}, return to normal operation

Table 8⑩ – Program Byte Flow

Step	Pin Number	Pin Name	Action
0	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A = V_{IH}, MODE B = V_{IL}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA(0-3)	Set next term group address (See Table 7)
5	12-19	IAD(0-7)	Set next input line address (See Table 4-5)
6	9	SEC/OD	Set to V_{IH}
7	11	ALE/ERA	Set to V_{IH} (Latch Address)
8	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
9	4	PVP	Set to V_{HH2}
10	11	ALE/ERA	Set to V_{IL}
11	9	SEC/OD	Set to V_{IL}
12	12-19	IAD(0-7)	Read data “Fuse State” byte (See Table 7)
13	4	PVP	Set to V_{IL}
14	---	---	Repeat step 5 – 13 until all 36 input lines and 1 macrocell line have been read
15	---	---	Repeat step 4 - 14 until all 10 term groups have been read
16	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
17	1	PVE	Set to V_{IL}, return to normal operation

Table 9⑩ - Verify Byte Flow

Step	Pin Number	Pin Name	Action
0	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A = V_{IL}, MODE B = V_{IL}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA(0-3)	Set term group address to 0h
5	12-19	IAD(0-7)	Set input line address to 00h
6④	11	ALE/ERA	Set to V_{HH2} (Enable Erase)
7	4	PVP	Set to V_{HH2} (See t_{RP}, t_{WP}), set to V_{IL}
8④	11	ALE/ERA	Set to V_{IL}
9	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
10	1	PVE	Set to V_{IL}, return to normal operation

④ Pin 11 (ALE/ERA) may follow pin 4 (PVP) as an alternative to steps 6 and 8.

Table 10⑩ – Erase All Flow

Step	Pin Number	Pin Name	Action
0	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
1	1	PVE	Set to V_{HH1}
2	2-3	MODE A-B	Set MODE A = V_{IH}, MODE B = V_{IH}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA(0-3)	Set term group address 0h
5	12-19	IAD(0-7)	Set input line address to 00h
6	11	ALE/ERA	Set to V_{IH} (Latch Address)
7⑤	9	SEC/OD	Set to V_{HH2} (Enable Security Mode)
8	4	PVP	Set to V_{HH2} (See t_{RP}, t_{WP}), set to V_{IL}
9⑤	9	SEC/OD	Set to V_{IL}
10	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
11	1	PVE	Set to V_{IL}, return to normal operation

⑤ Pin 9 (SEC/OD) may follow Pin 4 (PVP) as an alternative to steps 7 and 9.

Table 11⑩ – (Set) Security Bit Flow

Step	Pin Number	Pin Name	Action
0	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
1	1	PVE	Set to V_{HH1}
2	2-3-	MODE A-B	Set MODE A = V_{IL}, MODE B = V_{IH}
3	11	ALE/ERA	Set to V_{IL}
4	5-8	TGA(0-3)	Set term group address to 0h
5	12-19	IAD(0-7)	set input line address to FFh
6	4	PVP	Set to V_{HH2} (See t_{RP}, t_{WP}), set to V_{IL}
7	12-19	IAD(0-7)	Set to high impedance (Hi – Z)
8	1	PVE	Set to V_{IL}, return to normal operation

Table 12⑩ – Program (Write) All Flow

6.0 PROGRAM /VERIFY (DC AND AC) PARAMETERS AND WAVEFORMS

Absolute Maximum Ratings

Voltages relative to ground (pin 1) +17.0V to –0.5V
(all other pins) +6.0V to –0.5V

DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
Vcc	Programming Supply Voltage	---	4.75	5.25	V
V_{HH}	Program/Verify Voltage 1	---	11.5	13	V
V_{HH2}	Program/Verify Voltage 2	---	15	16⑥	V
V_{HH3}	Program/Verify Voltage 3	---	---	10	V
I_{CC}	Supply Current	Program/Verify	---	100	mA
V_{IL}	Input voltage Low	---	---	.80	V
V_{IH}	Input Voltage High	---	2	V_{CC} + 0.3	V
V_{OL}	Output Voltage Low	I_{OL} = +8.0mA	---	0.5	V
V_{OH}	Output Voltage high	I_{OH} = +4.0mA	2.4	---	V
I_{LI}	Input Leakage Current	GND<V_{IN}<V_{CC}MAX	---	10⑦	µA
I_{LO}	Output Leakage Current	GND<V_{IN}<V_{CC}MAX	---	10	µA

⑥ ICT recommend using 15.50V with a tolerance of 0.50V.

⑦ I_{LI} (Input Leakage Current) is 100 µA for Pins 1, 4, 9 and 11 on the range V_{CC}<V_{IN}<V_{HH}, 2 and 3.

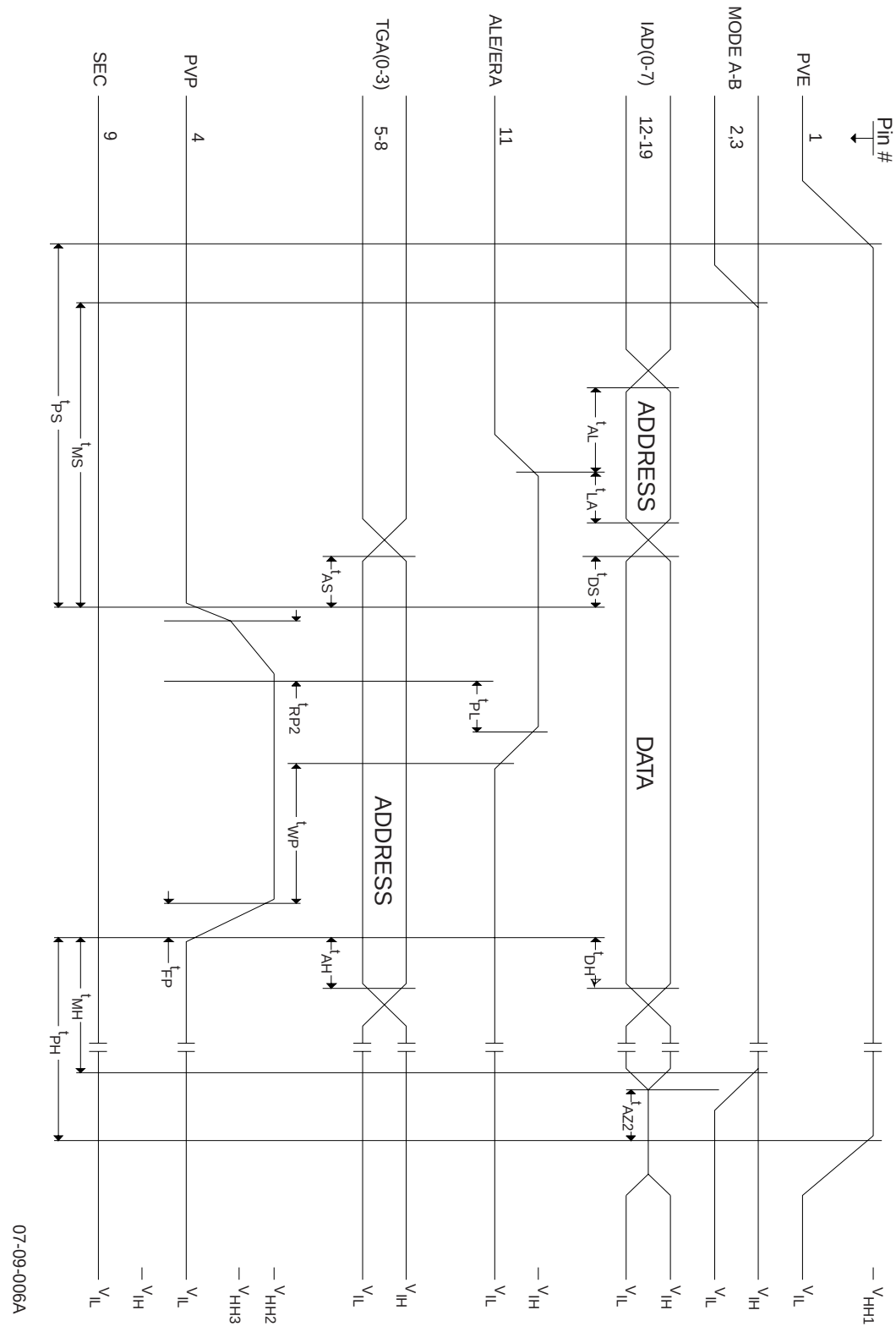
AC Electrical Characteristics

Symbol	Parameter	Diagram ⑧	Min ⑨	Max	Units
$t_{AZ1,2}$	AD(0-7) Hi - Z set-up to PVE	P, V, E, S, W	1		µS
t_{PS}	PVE set-up to V_{PP}	P, V, E, S, W	4		µS
t_{MS}	mODE SET-UP TO V_{PP}	P, V, E, S, W	3		µS
t_{AL}	IAD Address set-up to ALE	P, V, E, S, W	1		µS
t_{LA}	IAD Address hold after ALE	P, V	1		µS
t_{DS}	IAD Data set-up to PVP	P	1		µS
t_{AZ3}	IAD Hi - Z before PVP	V	1		µS
t_{LS}	ALE set-up to PVP	E, S, W	1		µS
t_{AS}	TGA Address set-up to PVP	P, E, W	1		µS
t_{PL}	ALE hold after PVP	P, V	1		µS
t_{DE}	IAD Data Enable after PVP	v	0		µS
t_{LP}	ALE low set-up to PVP	P, V	1		µS
t_{SS}	SEC set-up to PVP	S	1		µS
t_{RP}	PVP^{1-2} rise time	P, E, S, W	50		µS/V
t_{WP}	PVP Program/Erase pulse width	P, E, W	10		mS
t_{SP}	PVP Security pulse width	S	300		mS
t_{VP}	PVP Verify pulse width	V	10		µS
t_{FP}	PVP fall time	P, V, E, S, W	1		µS
t_{DV}	IAD Data valid after PVP	V	1		µS
t_{DZ}	IAD Data Hi - Z after PVP	V	1		µS
t_{DH}	IAD Data hold after PVP	P	1		µS
t_{AH}	IAD Address hold after PVP	P, V	1		µS
t_{EH}	ERA, SEC, IAD, TGA, Mode after PVP	E, S, W	1		µS
t_{MH}	Mode hold after PVP	P, V	1		µS
t_{PH}	PVE hold after PVP	P, V, E, S, W	1		µS
t_{SOD}	OD set-up to output disable	V	2		µS
t_{HOD}	OD hold for output disable	V	1		µS

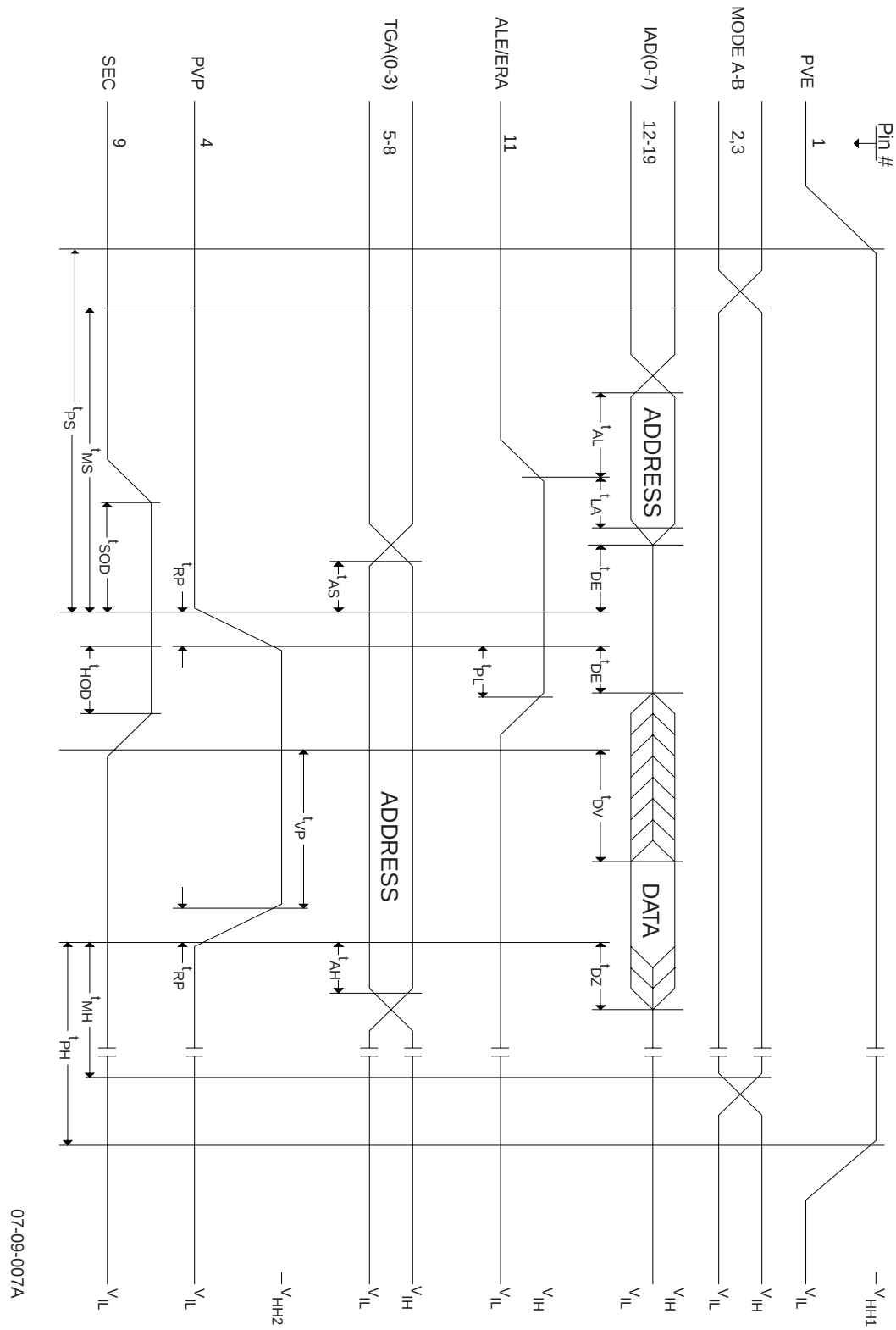
⑧ Identifies the associate waveform timing diagram(s) to timing parameter:

PB = Program Byte
V = Verify Byte
E = Erase All
S = Set Security Bit
W = Write All

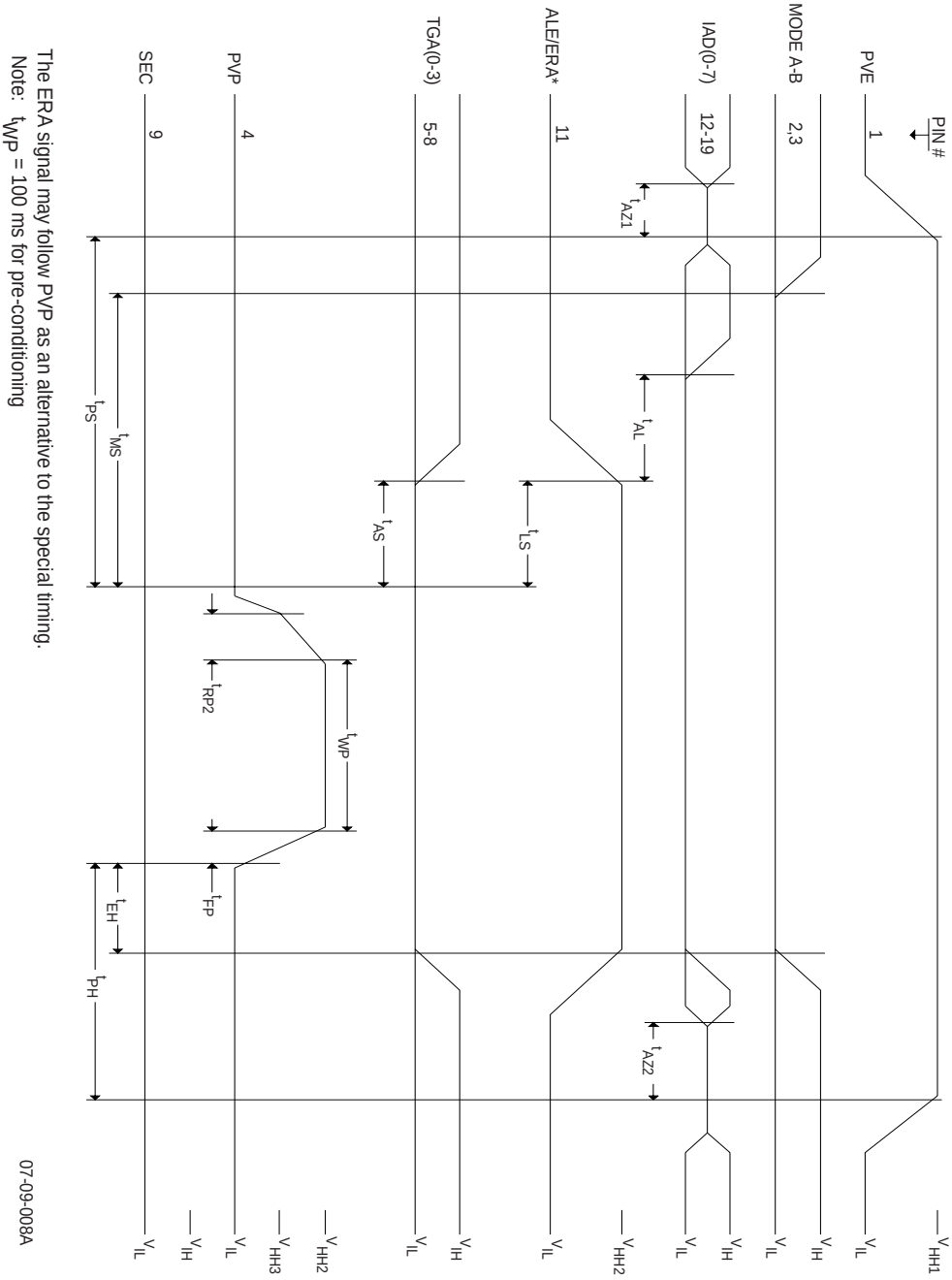
⑨ All Timings are measured at 10% and 90% rise and fall points.



Program Byte Waveforms (Mode A=1 and Mode B=1)

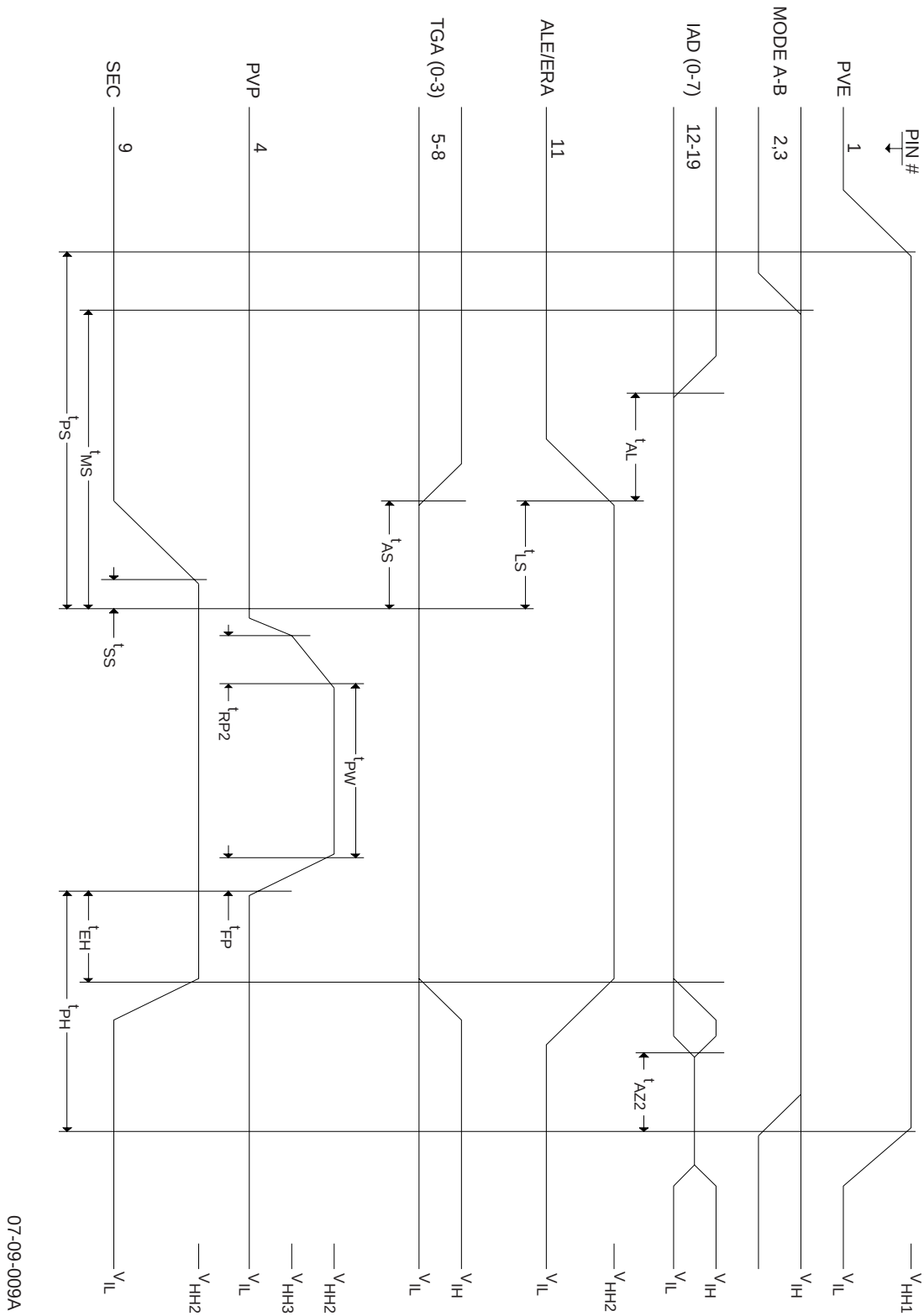


Verify Byte Waveforms (Mode A=1 and Mode B=0)

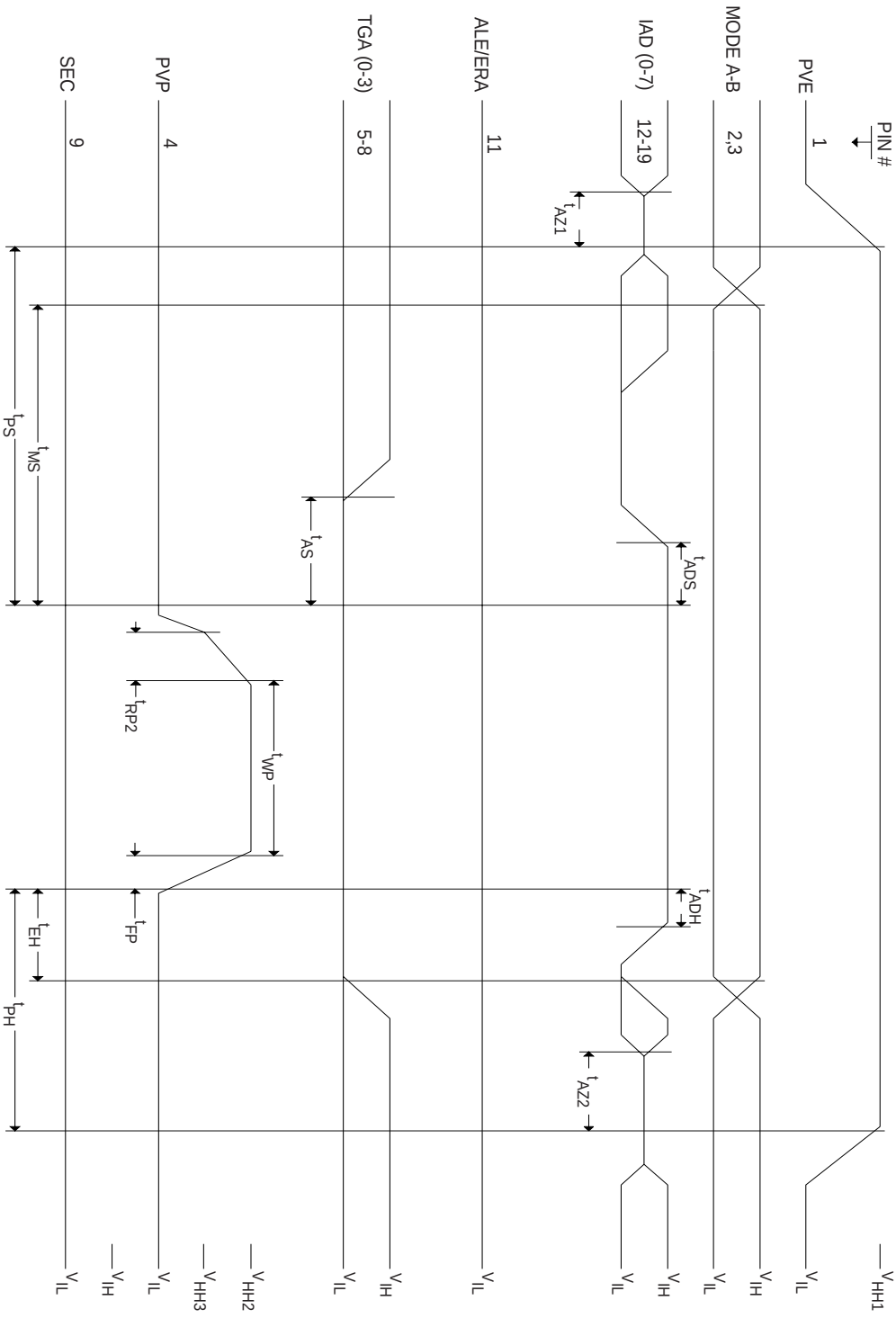


The ERA signal may follow PVP as an alternative to the special timing.
Note: t_{WP} = 100 ms for pre-conditioning

Erase All Waveforms (Mode A=0 and Mode B=0)



Set Security Bit (Mode A=1 and Mode B=1)



t_{ADS} = 1 us (min) and t_{ADH} = 1 us (min).
t_{WP} = 100 ms for pre-conditioning.

Program (Write) All Waveforms (Mode A=0 and Mode B=1)

7.0 NOTES AND COMMENTS

1. The rise time for PVP during Program/Verify and Security Bit is different.
   Please see the flowchart individually for detail. (Reference Page 14).
   H1 = VHH1
   H2 = VHH2
   X = VIL or VIH (TTL Don't Care)
   0 = VIL (TTL Low)
   1 = VIH (TTL High)
   ^1= High Level Latch

2. "FB #" means FeedBack from the Macrocell # (the "#" corresponds to the pin number).
   (Reference page 15).

3. All data programmed to the IAD(0-7) pins must first be inverted from its state in JEDEC fuse map. Data read (verified) from the IAD(0-7) pins, howere, does not require any inversion for correct correspondence to the fuse map values. (Reference page 16).
   MSB = Most Significant Bit
   LSB = Least Significant Bit
   X = TTL Don't Care
   R = Factory reserved
   D, C, B and A = Macrocell Configuration Bits

4. Pin 11 (ALE/ERA) may follow pin 4 (PVP) as an alternative to steps 6 and 8. (Reference page 18).

5. Pin 9 (SEC/OD) may follow Pin 4 (PVP) as an alternative to steps 7 and 9. (Reference page 18).

6. ICT recommend using 15.50V with a tolerance of 0.50V. (Reference page 19).

7. I_{LI} (Input Leakage Current) is 100 mA for Pins 1, 4, 9 and 11 on the range $V_{CC}<V_{IN}<V_{HH}$, 2 and 3.
   (Reference page 19).

8. Identifies the associate waveform timing diagram(s) to timing parameter:
   (Reference page 20).
   PB = Program Byte V = Verify Byte
   E = Erase All S = Set Security Bit
   W = Write All

9. All Timings are measured at 10% and 90% rise and fall points. (Reference page 20).

10. All pin numbers in diagrams and tables refer to the PDIP package unless stipulated in the title.
    (Reference pages 7-9 and 14-18).