MACHINE INSTRUCTIONS

Symbol	Function	Details	Addressing mode													
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
ADC (Note 1) (Note 9)	When T=0 A←A+M+C	Adds the carry accumulator and memory contents. The results are entered into the accumulator				69	2	2							65	3	2			
	When T=1 M(X)←M(X)+M+C	Adds the contents of the memory in the address indicated by index register X, the contents of the memory specified by the addressing modes in the columns on the right, and the contents of the carry. The results are entered into the memory at the address indicated by index register X.																		
AND (Note 1)	When T=0 A←A∧M	"AND-s" the accumulator and memory contents. The results are entered into the accumulator.				29	2	2							25	3	2			
	When T=1 M(X)←M(X)∧M	"AND-s" the contents of the memory of the address indicated by index register X and the contents of the memory specified by the addressing modes in the columns on the right. The results are entered into the memory at the address indicated by index register X.																		
ASL	7 0 C ← [ ] ←0	1-bit shifts the contents of accumulator or contents of memory to the left. "0" enters 0th bit of memory or accumulator and the contents of the 7th bit enter carry flag.							0A	2	1				06	5	2			
BBC (Note 4)	A_b or M_b=0?	Branches when the contents of the bit specified in the accumulator or memory are "0".										13+2i	4	2				17+2i	5	3
BBS (Note 4)	A_b or M_b=1?	Branches when the contents of the bit specified in the accumulator or memory are "1"										03+2i	4	2				07+2i	5	3
BCC (Note 4)	C=0?	Branches when the contents of carry flag are "0"																		
BCS (Note 4)	C=1?	Branches when the contents of carry flag are "1".																		
BEQ (Note 4)	Z=1?	Branches when the contents of zero flag are "1".																		
BIT	A∧M	"AND-s" the contents of accumulator and memory. The results are not entered anywhere.													24	3	2			
BMI (Note 4)	N=1?	Branches when the contents of negative flag are "1".																		
BNE (Note 4)	Z=0?	Branches when the contents of zero flag are "0"																		
BPL (Note 4)	N=0?	Branches when the contents of negative flag are "0"																		
BRA	PC←PC±offset	Jumps to address where offset has been added to the program counter.																		
BRK	B←1 $M(S)←PC_H$ S←S−1 $M(S)←PC_L$ S←S−1 M(S)←PS S←S−1 $PC_L←AD_L$ $PC_H←AD_H$	Executes software interrupt.	00	7	1															

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Addressing mode																												Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
75	4	2				6D	4	3	7D	5	3	79	5	3							61	6	2	71	6	2							N	V	•	•	•	•	Z	C
35	4	2				2D	4	3	3D	5	3	39	5	3							21	6	2	31	6	2							N	•	•	•	•	•	Z	•
16	6	2				0E	6	3	1E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																												90	2	2			•	•	•	•	•	•	•	•
																												B0	2	2			•	•	•	•	•	•	•	•
																												F0	2	2			•	•	•	•	•	•	•	•
						2C	4	3																									M_7	M_6	•	•	•	•	Z	•
																												30	2	2			•	•	•	•	•	•	•	•
																												D0	2	2			•	•	•	•	•	•	•	•
																												10	2	2			•	•	•	•	•	•	•	•
																												80	4	2			•	•	•	•	•	•	•	•
																																	•	•	•	1	•	1	•	•

Symbol	Function	Details	Addressing mode																			
			IMP			IMM			A			BIT,A			ZP			BIT,ZP				
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#		
BVC (Note 4)	V=0?	Branches when the contents of overflow flag are "0."																				
BVS (Note 4)	V=1?	Branches when the contents of overflow flag are "1."																				
CLB	A_b or M_b←0	Clears the contents of the bit specified in the accumulator or memory to "0"										1B+2i	2	1				1F+2i	5	2		
CLC	C←0	Clears the contents of the carry flag to "0"	18	2	1																	
CLD	D←0	Clears the contents of decimal mode flag to "0."	D8	2	1																	
CLI	I←0	Clears the contents of interrupt disable flag to "0."	58	2	1																	
CLT	T←0	Clears the contents of X-modified arithmetic mode flag to "0"	12	2	1																	
CLV	V←0	Clears the contents overflow flag to "0"	B8	2	1																	
CMP (Note 3)	When T=0 A−M When T=1 M(X)−M	Compares the contents of accumulator and memory. Compares the contents of the memory specified by addressing modes in the columns on the right with the contents of the address indicated by index register X				C9	2	2							C5	3	2					
COM	M←M	Formes one's complement of contents of memory, and store it into memory.													44	5	2					
CPX	X−M	Compares the contents of index register X and memory				E0	2	2							E4	3	2					
CPY	Y−M	Compares the contents of index register Y and memory				C0	2	2							C4	3	2					
DEC	A←A−1 or M←M−1	Decrements the contents of accumulator or memory by 1.							1A	2	1				C6	5	2					
DEX	X←X−1	Decrements the contents of index register X by 1.	CA	2	1																	
DEY	Y←Y−1	Decrements the contents of index register Y by 1	88	2	1																	
DIV (Note 8)	A←(M(zz+X+1), M(zz+X))/A M(S) ← 1's complement of Remainder S←S− 1	Divides by accumulator the 16-bit data that is the contents of M(zz+x+1) for high byte and the contents of the next address memory for low byte and stores the quotient in the accumulator and the remainder on the stack as 1's complement																				
EOR (Note 1)	When T=0 A←A¥M When T=1 M(X)←M(X)¥M	"Exclusive-ORs" the contents of accumulator and memory The results are stored into the accumulator. "Exclusive-ORs" the contents of the memory specified by the addressing modes in the columns on the right and the contents of the memory at the address indicated by index register X. The results are stored into the memory at the address indicated by index register X.				49	2	2							45	3	2					
FST (Note 5)		Connects oscillator output to X_{OUTF}	E2	2	1																	
INC	A←A+1 or M←M+1	Increments the contents of accumulator or memory by 1							3A	2	1				E6	5	2					
INX	X←X+1	Increments the contents of index register X by 1	E8	2	1																	
INY	Y←Y+1	Increments the contents of index register Y by 1	C8	2	1																	

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Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																											50	2	2				•	•	•	•	•	•	•	•
																											70	2	2				•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	0
																																	•	•	•	•	0	•	•	•
																																	•	•	•	•	•	0	•	•
																																	•	•	0	•	•	•	•	•
																																	•	0	•	•	•	•	•	•
D5	4	2				CD	4	3	DD	5	3	D9	5	3							C1	6	2	D1	6	2							N	•	•	•	•	•	Z	C
																																	N	•	•	•	•	•	Z	•
						EC	4	3																									N	•	•	•	•	•	Z	C
						CC	4	3																									N	•	•	•	•	•	Z	C
D6	6	2				CE	6	3	DE	7	3																						N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
E2	16	2																															•	•	•	•	•	•	•	•
55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2							N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
F6	6	2				EE	6	3	FE	7	3																						N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode											
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
JMP	If addressing mode is ABS $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is IND $PC_L \leftarrow (AD_H, AD_L)$ $PC_H \leftarrow (AD_H, AD_L+1)$ If addressing mode is ZP, IND $PC_L \leftarrow (00, AD_L)$ $PC_H \leftarrow (00, AD_L+1)$	Jumps to new address																		
JSR	$M(S) \leftarrow PC_H$ $S \leftarrow S-1$ $M(S) \leftarrow PC_L$ $S \leftarrow S-1$ After executing the above, if addressing mode is ABS, $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is SP, $PC_L \leftarrow AD_L$ $PC_H \leftarrow FF$ If addressing mode is ZP IND, $PC_L \leftarrow (00, AD_L)$ $PC_H \leftarrow (00, AD_L+1)$	After storing contents of program counter in stack, and jumps to new address																		
LDA (Note 2)	When T=0 A←M When T=1 M(X)←M	Load accumulator with contents of memory Load memory indicated by index register X with contents of memory specified by addressing mode shown in right column.				A9	2	2							A5	3	2			
LDM	M←IMM	Load memory with immediate value													3C	4	3			
LDX	X←M	Load index register X with contents of memory				A2	2	2							A6	3	2			
LDY	Y←M	Load index register Y with contents of memory				A0	2	2							A4	3	2			
LSR	7 0 0 → ▯ → C	Shift the contents of accumulator or memory to the right by one bit. 0th bit of accumulator or memory is stored in carry, 7th bit is cleared.							4A	2	1				46	5	2			
MUL (Note 8)	M(S)·A←AXM(zz+X) S←S−1	Multiplies accumulator with the memory specified by the zero page X addressing mode and stores the high byte of the result on the stack and the low byte in the accumulator.																		
NOP	PC←PC+1	No operation	EA	2	1															
ORA (Note 1)	When T=0 A←AVM When T=1 M(X)←M(X)VM	Produce the logical OR of the contents of memory and accumulator. The result is stored in accumulator. produce the logical OR of contents of memory indicated by index register X and contents of memory specified by addressing mode shown in right column. The result is stored in memory of address specified by index register X.				09	2	2							05	3	2			

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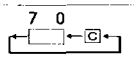
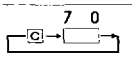
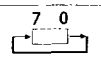
Addressing mode																								Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
						4C	3	3							6C	5	3	B2	4	2													•	•	•	•	•	•	•	•
						20	6	3										02	7	2										22	5	2	•	•	•	•	•	•	•	•
B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2							N	•	•	•	•	•	Z	•
																																•	•	•	•	•	•	•	•
			B6	4	2	AE	4	3				BE	5	3																			N	•	•	•	•	•	Z	•
B4	4	2				AC	4	3	BC	5	3																					N	•	•	•	•	•	Z	•
56	6	2				4E	6	3	5E	7	3																					0	•	•	•	•	•	Z	C
62	15	2																														•	•	•	•	•	•	•	•
																																•	•	•	•	•	•	•	•
15	4	2				0D	4	3	1D	5	3	19	5	3							01	6	2	11	6	2							N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																		
			IMP			IMM			A			BIT,A			ZP			BIT,ZP			
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
PHA	M(S)←A S←S−1	Saves the contents of the accumulator in the memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1.	48	3	1																
PHP	M(S)←PS S←S−1	Saves the contents of processor status register in the memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1	08	3	1																
PLA	S←S+1 A←M(S)	Increments the contents of stack pointer by 1 and pulls from the memory at the address indicated by the stack pointer, and store it in accumulator.	68	4	1																
PLP	S←S+1 PS←M(S)	Increments the contents of stack pointer by 1 and pulls from the memory at the address indicated by the stack pointer. and store it in processor status register	28	4	1																
ROL		Connects the carry flag and the accumulator or memory and rotates the contents to the left by 1 bit.							2A	2	1				26	5	2				
ROR		Connects the carry flag and the accumulator or memory and rotates the contents to the right by 1 bit.							6A	2	1				66	5	2				
RRF		Rotates the contents of memory to the right by 4 bits.													82	8	2				
RTI	S←S+1 PS←M(S) S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from the interrupt routine to the main routine.	40	6	1																
RTS	S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from the subroutine to the main routine.	60	6	1																
SBC (Note 1) (Note 9)	When T=0 A←A−M−C When T=1 M(X)←M(X)−M−C	Subtracts the contents of memory and carry flag from the contents of accumulator. The results are stored into the accumulator. Subtracts contents of carry flag and contents of the memory indicated by the addressing modes shown in the columns on the right from the memory at the address indicated by index register X. The results are stored into the memory of the address indicated by index register X.				E9	2	2							E5	3	2				
SEB	A_b or M_b←1	Sets the specified bit contents of accumulator or memory to "1."										0B+2i	2	1				0F+2i	5	2
SEC	C←1	Sets the contents of carry flag to "1."	38	2	1																
SED	D←1	Sets the contents of decimal mode flag to "1."	F8	2	1																
SEI	I←1	Sets the contents of interrupt disable flag to "1."	78	2	1																
SET	T←1	Sets the contents of X-modified arithmetic mode flag to "1."	32	2	1																
SLW (Note 5)		Releases the connection between the oscillator output and pin X_{OUTF}.	C2	2	1																

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Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																																•	•	•	•	•	•	•	•
																																•	•	•	•	•	•	•	•
																																N	•	•	•	•	•	Z	•
																																(Value saved in stack)							
36	6	2				2E	6	3	3E	7	3																					N	•	•	•	•	•	Z	C
76	6	2				6E	6	3	7E	7	3																					N	•	•	•	•	•	Z	C
																																•	•	•	•	•	•	•	•
																																(Value saved in stack)							
																																•	•	•	•	•	•	•	•
F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2							N	V	•	•	•	•	Z	C
																																•	•	•	•	•	•	•	•
																																•	•	•	•	•	•	•	1
																																•	•	•	•	1	•	•	•
																																•	•	•	•	•	1	•	•
																																•	•	1	•	•	•	•	•
																																•	•	•	•	•	•	•	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
STA	M←A	Stores the contents of accumulator in the memory.													85	4	2			
STP (Note 7)		Stops the oscillation of the oscillator.	42	2	1															
STX	M←X	Stores the contents of index register X in the memory.													86	4	2			
STY	M←Y	Stores the contents of index register Y in the memory.													84	4	2			
TAX	X←A	Transfers the contents of accumulator to index register X.	AA	2	1															
TAY	Y←A	Transfers the contents of accumulator to index register Y.	A8	2	1															
TST	M=0?	Tests whether the contents of memory are "0" or not.													64	3	2			
TSX	X←S	Transfers the contents of stack pointer to index register X.	BA	2	1															
TXA	A←X	Transfers the contents of index register X to the accumulator.	8A	2	1															
TXS	S←X	Transfers the contents of index register X to the stack pointer.	9A	2	1															
TYA	A←Y	Transfers the contents of index register Y to the accumulator.	98	2	1															
WIT (Note 6)		Stops the internal clock.	C2	2	1															

Note 1 : The number of cycles "n" is added by 3 when T is 1.
2 : The number of cycles "n" is added by 2 when T is 1.
3 : The number of cycles "n" is added by 1 when T is 1.
4 : The number of cycles "n" is added by 2 when branching has occurred.
5 : This instruction is not for any other models than M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP and M50758-XXXSP.
6 : This instruction is not provided for M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, and M50758-XXXSP.
7 : This instruction is not provided for M50752-XXXSP, M50757-XXXSP and M50758-XXXSP.
8 : This instructions are not supported by all models. For details, refer to the description of functions of each model.
9 : N, V and Z flags are invalid at decimal operation mode.

Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2							•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
			96	5	2	8E	5	3																									•	•	•	•	•	•	•	•
94	5	2				8C	5	3																									•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•

Symbol	Contents
IMP	Implied addressing mode
IMM	Immediate addressing mode
A	Accumulator or Accumulator addressing mode
BIT, A	Accumulator bit relative addressing mode
ZP	Zero page addressing mode
BIT, ZP	Zero page bit relative addressing mode
ZP, X	Zero page X addressing mode
ZP, Y	Zero page Y addressing mode
ABS	Absolute addressing mode
ABS, X	Absolute X addressing mode
ABS, Y	Absolute Y addressing mode
IND	Indirect absolute addressing mode
ZP, IND	Zero page indirect absolute addressing mode
IND, X	Indirect X addressing mode
IND, Y	Indirect Y addressing mode
REL	Relative addressing mode
SP	Special page addressing mode
C	Carry flag
Z	Zero flag
I	Interrupt disable flag
D	Decimal mode flag
B	Break flag
T	X-modified arithmetic mode flag
V	Overflow flag
N	Negative flag

Symbol	Contents
+	Addition
−	Subtraction
∧	Logical OR
∨	Logical AND
∀	Logical exclusive OR
—	Negation
←	Shows direction of data flow
X	Index register X
Y	Index register Y
S	Stack pointer
PC	Program counter
PS	Processor status register
PC_H	8 high-order bits of program counter
PC_L	8 low-order bits of program counter
AD_H	8 high-order bits of address
AD_L	8 low-order bits of address
(AD_H, AD_L)	Contents of memory at address indicated by AD_H and AD_L, in AD_H is 8 high-order bits and AD_L is 8 low-order bits.
$(00, AD_L)$	Contents of address indicated by zero page AD_L
FF	FF in Hexadecimal notation
M	Memory specified by address designation of any addressing mode
M (X)	Memory of address indicated by contents of index register X
M (S)	Memory of address indicated by contents of stack pointer
A_b	1 bit of accumulator
M_b	1 bit of memory
OP	Opcode
n	Number of cycles
#	Number of bytes