A Predictive Current Control Scheme for a Hybrid AC/AC Direct Power Converter

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Abstract

The Hybrid ac/ac Direct Power Converter (HDPC) has the advantage of improved voltage transfer ratio and higher robustness against supply voltage unbalances over the Conventional Matrix Converters (CMC). The HDPC also has the inherent advantages of the CMC such as: adjustable input power factor, sinusoidal supply currents and no bulky energy storage elements which reduce the life time of the converter. This paper proposed a predictive current controller scheme for a HDPC based on 2-stage matrix converter providing unity voltage transfer ratios; even in the case the supply voltage is highly unbalanced. The proposed predictive current controller is simple in digital implementation, provides higher bandwidth control, requires no additional circuitry and maintains a constant switching frequency which allows synchronizing the switching of the HDPC for sinusoidal supply currents.

1 Introduction

AC/AC Direct Power Converters (DPC) deliver variable frequency variable voltage to a load without using any intermediate energy storage devices. Matrix Converters (MC) offer sinusoidal supply currents, adjustable input displacement power factor irrespective of the type of the load and bidirectional power flow apart from being a DPC [1]-[6]. Absence of energy storage devices such as electrolytic capacitors enables the MC to increase its power density and to offer longer life span. Two of the promising MC structures for three-phase to three-phase DPC are shown in Fig. 1: shows the single stage MC Fig. 1(a) and shows the two-stage MC Fig. 1(b).

Two stage MC [7]-[10], also referred in the literature as, the 'dual bridge MC' [8], 'indirect matrix converter' or the 'sparse matrix converter' [9], offers the possibility to reduce the number of semiconductor devices compared to the single stage MC while maintaining the similar input/output performance. Two-stage MC structure shown in Fig. 1(b) consists of a three phase to two phase matrix converter operates as a Current Source type Rectifier (CSR) which is connected to a conventional Voltage Source type Inverter (VSI). The intermediate link between the CSR and VSI is a fast fluctuating voltage DC link due the absence of any energy storage device. Therefore, synchronization of the switching instances for the CSR and the VSI is highly important in order to obtain sinusoidal supply currents. Furthermore, the absence of any energy storage elements in these DPCs requires having a clamp circuit to protect the converter (not shown in Fig. 1) during sudden turn off of the load due to over current situation. In case of single stage CMC, twelve additional diodes and a clamp capacitor should be employed [4,5], while a two-stage MC requires only one diode and a capacitor connected to the intermediate DC link [9,10].

Voltage Transfer Ratio (VTR), which is the ratio of load voltage over the supply, is theoretically limited to 0.866 in the case of MC. In practice this figure could further reduce due to supply voltage disturbances, voltage drop in the semiconductor devices, pulse width limitation due to 4-step commutation times or dead times and also due to voltage drops in the filter. In the case of supply voltage unbalances the maximum undistorted load voltage capability is further reduced. Improvement in VTR can be obtained using active or passive compensation techniques [12]. Despite its advantages, the reduced VTR in MC prevents it from feeding standard motors whereas more expensive customized motors will have to be

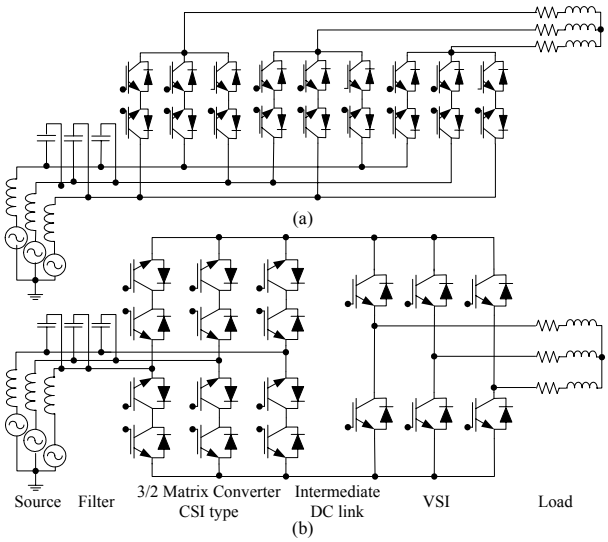

Fig.1. Matrix converter structures: (a) single stage CMC, (b) two-stage MC

utilized. This factor has been a key issue when commercializing a MC based drive. A traditional boost type back to back VSI which is not very expensive could solve these problems by employing a large DC link capacitor to store energy required to compensate those effects. On the other hand using electrolytic capacitors in the dc link could degrade the lifespan of the converter and reduce the power density. Therefore, it is important to investigate alternative converter structures such as the DPC which has unity load voltage transfer to replace the traditional drives providing the possibility to have cost effective, compact industrial motor drives while fulfilling the standard power quality regulations.
Hybrid Direct Power Converter (HDPC) structures as proposed in [13] offer improved robustness to supply voltage variations and provide unity VTR, which overcome the main draw back of CMC. In this paper, a new predictive current controller for a HDPC based on two-stage MC topology is proposed. The proposed control structure allows using the fixed frequency pulse width modulation therefore synchronization of switching of the AVS can be achieved to maintain the sinusoidal input currents. The predictive control also offers simple DSP based digital control without requiring any external circuitry like in the case of hysteresis current controller [13]. The paper presents an analytical study, control technique, modulation scheme and the important details of a realistic simulation model and simulation results of the proposed control scheme for HDPC.

2. Hybrid direct power converter

2.1 Structure of HDPC

The proposed HDPC structure is based on adding an Auxiliary Voltage Source (AVS) in the intermediate dc link of the two-stage MC, as suggested in Fig.2a in order to boost up the average dc-link voltage seen by the inverter stage. It is required that this AVS should provide higher voltage magnitude than any line to line supply voltage. Therefore, when the converter demands a higher load voltage than the theoretical maximum, the AVS will kick in increasing dc link voltage. One of the possible arrangements for this AVS is shown in Fig. 2 (b) where a simple boost type converter is charging the AVS capacitor. AVS utilizes additional TR_3 and TR_4 switches to commutate the currents to the VSI from both the AVS and the rectification stage, as required. It can also be noticed that inductor (L_{AUX}) and capacitor (C_{AUX}) in the AVS store energy, as a result, could endanger the concept of direct power conversion. Therefore, the value of the C_{AUX} and L_{AUX} has to be minimized. This is achieved by keeping the AVS voltage (V_{AUX}) constant by controlling the current through the boost inductor (i) so that an accurate balance of input and output power over a switching period is achieved. Additionally, C_{AUX} in the AVS can also act as a clamp capacitor to absorb the inductive energy from the load when

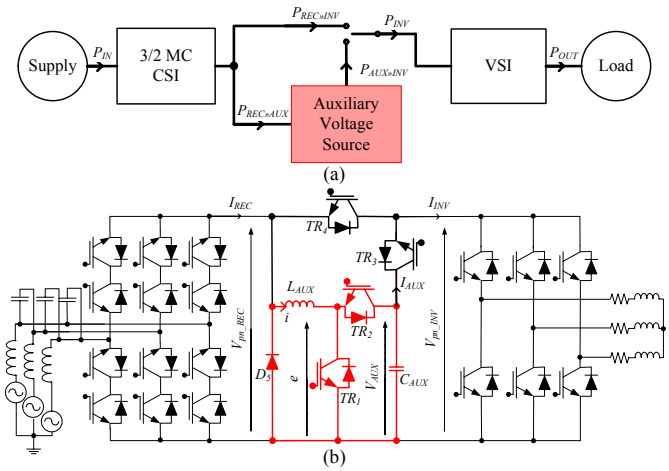

Fig.2. Proposed hybrid DPC: (a) Principal Model, (b) One of the promising arrangements with an auxiliary boost converter connected in the intermediate

the inversion stage needs to be turned off due to an over current situation. Therefore, additional components for clamp circuitry are not required unlike the case of CMC. In a regenerative situation, stored energy in the C_{AUX} could be fed back to the grid via the rectification stage by conducting TR_4 and TR_2, where the AVS acts as a buck type converter. Switch TR_3 will be utilized whenever the AVS is to be used to boost the dc link voltage seen by the VSI, where its switching will be determined by (6). An average current predictive controller scheme for controlling the AVS in the HDPC is proposed and the details will be explained separately.

2.2 Modulation strategy

Implementation of Space Vector Modulation (SVM) for a two-stage MC has been discussed in [9, 10] and [13]; a similar approach as in [10, 13] can be used for the HDPC. As shown in Fig. 3 the adjacent active input current vectors in a CSI type rectification stage (d_γ,d_δ) and adjacent active output voltage vectors in a VSI type inverter stage (d_α, d_β) can be expressed according to the SVM for two-stage MC as:

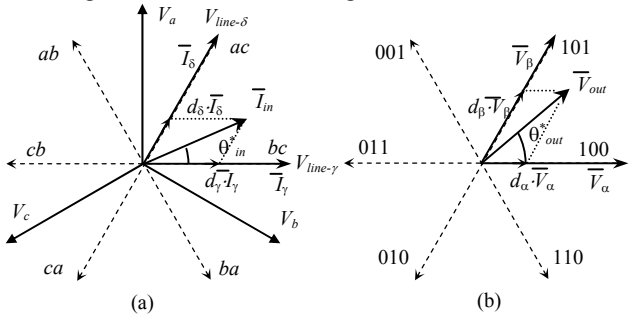

Fig.3. Generation of the reference vectors in a two-stage MC SVM: (a) rectification stage; (b) inversion stage.

$$d_\gamma = m_R \cdot \sin\left(\pi/3 - \theta^*_{in}\right) \qquad d_\delta = m_R \cdot \sin\theta^*_{in} \tag{1}$$

$$d_\alpha = m_I \cdot \sin\left(\pi/3 - \theta^*_{out}\right) \qquad d_\beta = m_I \cdot \sin\theta^*_{out} \tag{2}$$

where m_R and m_I are the rectification and inversion stage modulation indexes and θ^*_{in} and θ^*_{out} are the angles within their respective sectors of the input current and output voltage reference vectors. By eliminating the zero vectors in the rectification stage, the modified duty cycles of the rectification stage (d^R_γ, d^R_δ) can be found as:

$$d^R_\gamma = \frac{d_\gamma}{d_\gamma + d_\delta} \qquad d^R_\delta = \frac{d_\delta}{d_\gamma + d_\delta} \tag{3}$$

Elimination of zero vectors from the rectification stage will produce a time varying dc link voltage (V_{pn_REC}) which can be expressed as:

$$V_{pn\_REC} = d^R_\gamma . V_{line-\gamma} + d^R_\delta . V_{line-\delta} \tag{4}$$

If the duty-cycle of the AVS is d_{AUX}, the resultant dc link voltage seen by the inversion stage (V_{pn_INV}) can be stabilized as:

$$V_{pn\_INV} = (1 - d_{AUX}).V_{pn\_REC} + d_{AUX}.V_{AUX} = \sqrt{2}.V_{OUT} \tag{5}$$

Therefore, duty cycle of the TR_4 can be obtained by (6) where, V_{OUT} is the load voltage demand and V_{AUX} is the magnitude of the voltage of the AVS.

$$d_{AUX} = \left(\frac{\sqrt{2}V_{OUT} - V_{pn\_REC}}{V_{AUX} - V_{pn\_REC}} \right) \tag{6}$$

The inverter stage use a double-sided asymmetric PWM switching sequence 0_1-α-β-α-0_2, as shown in Fig. 4. The modulation index of the inversion stage can now be expressed as:

$$m_I = \frac{\sqrt{2}V_{OUT}}{V_{pn-INV}} \tag{7}$$

If the duty cycle of the TR_1 in the AVS is d corresponding duty ratios for $ON1$, ON_3, ON_2, OFF_1 and OFF_2 as shown in Fig. 4 can be obtained as follows:

$$\left\{ \begin{array}{l} d_{ON_1} = \frac{d^R_\gamma \cdot d}{2}, d_{ON_3} = \frac{d^R_\delta \cdot d}{2}, d_{ON_2} = d_{ON_1} + d_{ON_3} \\ d_{OFF_1} = d^R_\gamma - 2 \cdot d_{ON_1}, d_{OFF_2} = d^R_\delta - 2 \cdot d_{ON_3} \end{array} \right\} \tag{8}$$

2.3 Analysis of Hybrid Direct Power Converter

In order to determine the requirement for the inductor current

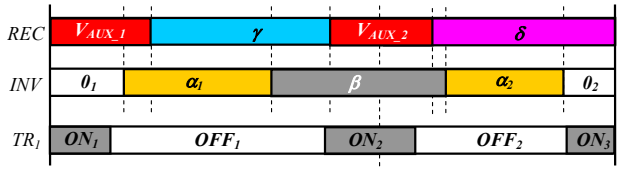

Fig.4. Combination of the switching state succession in HDPC: γ, δ are the active vectors of the rectification stage and α, β are the active vectors in the inversion stage, 0 are the inversion-stage zero vectors, ON and OFF instances corresponds to the switching of TR_1 in the AVS during one switching period.

controller, an analysis on the shape of the reference current is made which is valid for balanced or unbalanced supply voltage conditions. For an ideal situation the balance of power over one switching period (T) for HDPC is expressed in (9), with reference to Fig. 2a, where P_{INV} is the input power to the inversion stage, P_{AUX} is the power supplied by the AVS and $P_{REC\text{-}INV}$ is the power delivered to the inversion stage by the rectifier.

$$P_{INV} = P_{REC \to INV} + P_{AUX \to INV} \tag{9}$$

Equation (9) can be used to derive an expression for the current supplied by the AVS to the inversion stage (I_{AUX}) during T as:

$$I_{AUX} = \frac{d_{AUX}}{\{d_{AUX} + (1-k)\}} I_{INV} \tag{10}$$

Where, I_{INV} is the current drawn by the inverter and,

$$k = \frac{\sqrt{2}V_{OUT}}{V_{AUX}} \tag{11}$$

The energy storage in the AVS during T_{PWM} should be kept zero in order to maintain sinusoidal supply currents. Therefore, neglecting any losses;

$$P_{REC \to AUX} = P_{AUX \to INV} \tag{12}$$

where, $P_{REC\text{-}AUX}$ is the input power of the AVS. The reference inductor current i^* in order to satisfy (12) can be obtained as follows:

$$i^* = \frac{I_{AUX}.V_{AUX}}{V_{pn\_REC}} \tag{13}$$

In an ideal case, if the inductor current i exactly follow the reference given in (13), it will result in zero energy exchange with C_{AUX}. Also exact tracking of i^* will allow the total current drawn by the AVS to split equally between the three input phases thereby leading to sinusoidal supply currents. Any error in tracking the reference i^* would result in energy needing to be storage in C_{AUX}. A properly tuned controller will maintain the average error low therefore the average energy storage in C_{AUX} becomes very low while the AVS is acting as a quasi-direct power converter.

Figure 5 shows the behavior of the normalized i^* and its Fourier spectrum when the HDPC demands a unitary VTR. When the supply voltage is balanced the Fourier spectrum of the reference i^* has spread over nearly 3 kHz band (Fig 5b), where in case of 10% supply voltage unbalance situation results having even more dense spectrum (Fig. 5d). Therefore, a current controller with fast dynamics should be employed in order for exactly tracking the fast varying reference i^*. Hysteresis or predictive type current controller can be selected in this situation as they inherently high bandwidth controllers. As the hysteresis controller requires additional circuitry and has very little control over the switching of the devices which could result in high stresses and increased losses, a predictive current controller is much more suitable for the control of AVS

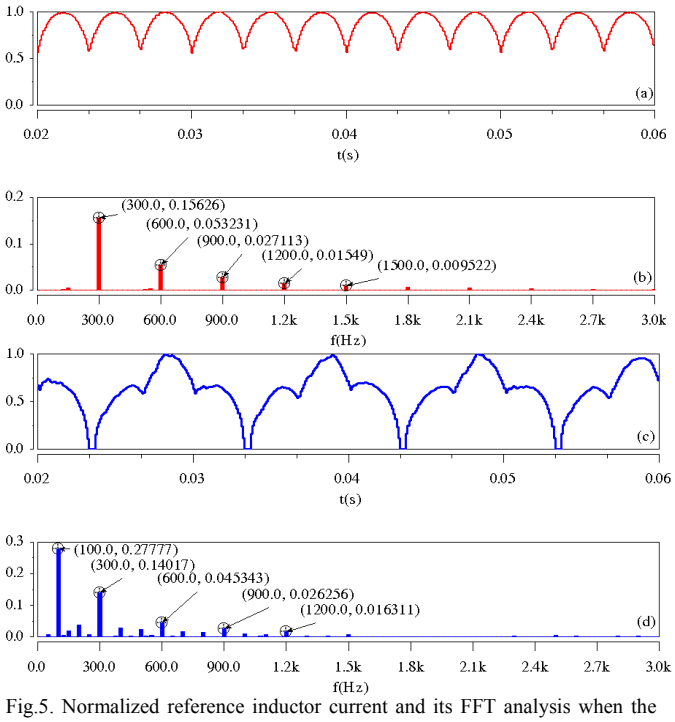

Fig.5. Normalized reference inductor current and its FFT analysis when the HDPC demands a Unitary VTR: (a, b) at balanced supply voltage, (c, d) at 10% supply voltage unbalance

in the HDPC because it will allow switching frequency of the AVS to be synchronized with the rectification and inversion stages as shown in Fig. 4.

It is also important to evaluate how much power is processed by the AVS compared to the total power of the converter as it will determine the cost of the required AVS. Assuming losses in the VSI are negligible compared to the load power P_{OUT}, which is assumed to be constant;

$$P_{OUT} = P_{INV} \tag{14}$$

By using (8), (9) and (13) the power processed by the AVS can be expressed as:

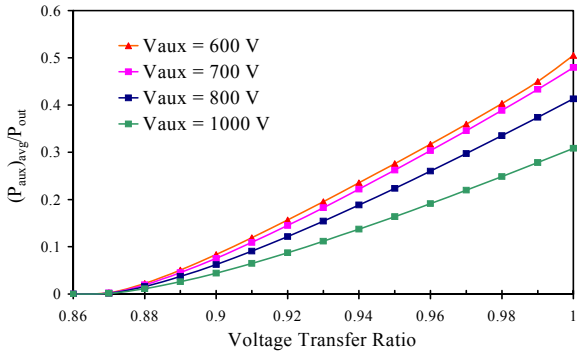

Fig.6. Variation of average power processed by the AVS in the intermediate dc link in the HDPC, as a fraction of the load power Vs the voltage transfer ratio at different level of auxiliary voltages.

$$P_{AUX} = \frac{d_{AUX}}{k.\{(1-k)+d_{AUX}\}} P_{OUT} \tag{15}$$

The average power processed by the AVS for different VTR demands at different V_{AUX} has been represented in Fig. 6 in order to estimate the power sharing of the HDPC. It indicates that the higher V_{AUX} the smaller the average power processed by the AVS thereby the smaller in size. But increasing V_{AUX} results in expensive high voltage devices in use for the AVS and VSI that potentially increases losses and the cost. Therefore, an intermediate level of 800 V is chosen that allows the use of 1200 V devices for both AVS and VSI where at unitary load voltage demand about 41% of the load power is processed by the AVS.

2.4. Control of hybrid direct power converter

It is a well known fact that matrix converter requires the use of high performance Digital Signal Processor (DSP) based control hardware to perform necessary calculations and bi-directional switch commutations as they are comparably more complex than other traditional power converter controls. Protection circuitry, A/D and D/A are also vital elements which could be incorporated must the control platform a compact solution. In addition to those essential elements, input voltage or output current zero crossing detectors will be used if the matrix converter switch commutation is based on input voltage or out put currents [6] respectively. As the basic control elements for HDPC are similar to matrix converter, control architecture used in two-stage MC [12] can be used. Four step supply voltage based commutation control [6] is used for the rectification stage of HDPC. The overall structure of the HDPC control as implemented in the simulation model is illustrated in Fig. 7. The details of two-stage MC control are omitted in this paper as it has been discussed in [10], [12]. Only the control of the predictive current control of AVS will be explained in the following section.

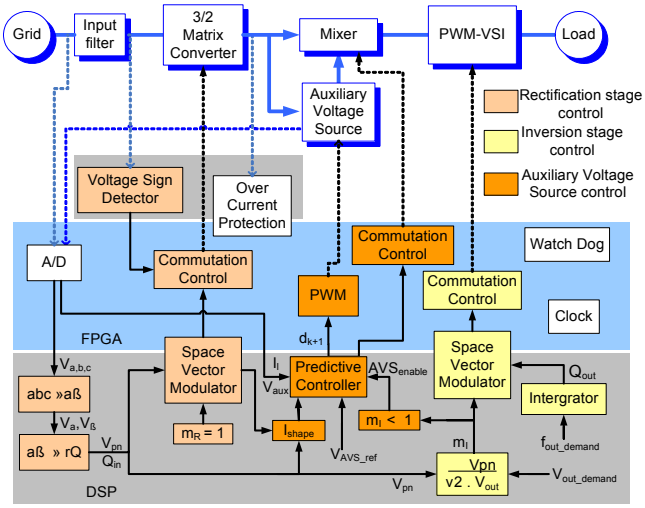

Fig.7. Control structure of the Hybrid Direct Power Converter

2.5 Predictive current controller for auxiliary voltage source

Controlling the current through the inductor L_{AUX} according to the i^* as described in (13) is the prime important in order to achieve sinusoidal supply currents with no energy storage in the AVS. A predictive current controller offers a possibility to make the average current trough L_{AUX} track the reference i^*. Therefore, the control architecture adopted for the AVS is shown in Fig.8 where a predictor for the current loop and a PI type voltage controller are used. The PI controller for the AVS capacitor voltage will produce the reference for inductive current magnitude.

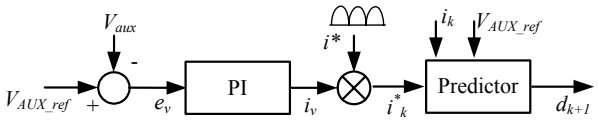

Fig.8. Structure of the predictive current controller of the AVS.

The following analysis shows details of the predictive current controller. With reference to Fig.2., the average voltage across the transistor TR_1 during a switching instant $k.T$, is e_k which can be expressed in terms of the voltage supply to the AVS (V_k), the reference current for the instant $(k+1)$and the sampled inductor current i_k as follows.

$$e_k = V_{pn\_REC_k} - L_{AUX} \cdot \frac{\left(i^*_{k+1} - i_k\right)}{T} - R_{AUX} . i_k \quad (16)$$

L_{AUX} and the R_{AUX} are the inductance and the resistance of the AVS inductor and T is the constant sampling period. Therefore the predicted voltage at the instant $(k+1)$ can be estimated as:

$$e_{k+1} = V_{pn\_REC_{k+1}} - L_{AUX} \cdot \frac{\left(i^*_{k+2} - i_{k+1}\right)}{T} - R_{AUX} . i_{k+1} \quad (17)$$

As the variation of the supply voltage to the AVS during one sampling interval can be assumed as a first order variation, the following first order Lagrange polynomial can be expressed as:

$$V_{pn\_REC_{k+1}} = 2 \cdot V_{pn\_REC_k} - V_{pn\_REC_{k-1}} \quad (18)$$

Accordingly a 2nd order Lagrange approximation can be used to express the reference current at instant $(k+2).T$ as follows:

$$i^*_{k+2} = 6 \cdot i^*_k - 8 \cdot i^*_{k-1} + 3 \cdot i^*_{k-2} \quad (19)$$

Equation (16) give rises to estimate the current thought the inductor at the instant $(k+1)$ as follows.

$$i_{k+1} = \frac{T}{L_{AUX}} \cdot \left[V_{pn\_REC_k} - e_k \right] + \left[1 - \frac{R_{AUX}}{L_{AUX}} \cdot T \right] \cdot i_k \quad (20)$$

Therefore, the duty ratio of the transistor TR_1 in the AVS at instant $(k+1).T$ can be predicted as follows:

$$d^*_{k+1} = \frac{V_{AUX\_ref} - e_{k+1}}{V_{AUX\_ref}} \quad (21)$$

Where, V_{AUX_ref} is the reference voltage set for the AVS capacitor which is selected as 800V.

3. Simulation Results

Operation of the HDPC, as explained in the section 2.4, was implemented using the Saber© simulation package. Fig.9 shows the operation of HDPC at unitary voltage transfer and 10% supply voltage unbalance. The simulation parameters are given in the appendix. According to Fig. 9(a) and Fig. 9(b), zero displacement of the supply voltage and the current could be observed as expected from the space vector modulation of the CSI type rectification stage with unity power factor. The waveform in Fig. 9(d) represents the filtered line-to-line load voltage where only the high frequency switching ripples have been eliminated to clearly observe the fundamental. The peak value of the filtered load voltage is about 590 V which proves that the voltage transfer is unity. At the same conditions, percentages of the supply current harmonics normalized to the magnitude of the fundamental frequency 50 Hz are shown in Fig. 10. Corresponding total harmonic distortion (THD) shows a maximum of 7.78 % with the first 20th harmonics.

The predicted current and the actual current of the AVS inductor when the supply is highly unbalanced is shown in Fig. 11 (top). Excellent tracking of the reference inductor current of the AVS indicates that the proposed predictive current controller yields a higher bandwidth control necessary for the sinusoidal supply currents. Fig. 11(bottom) shows that the dc link voltage produced by the HDPC is pulsating due to the absence of any energy storage unlike in the case of a conventional VSI. The maximum voltage value corresponds to the AVS capacitor voltage of 800V. In a HDPC, the AVS is kicking in only when the instantaneous load voltage demand cannot be fulfilled with the rectification stage. The reference inductor current falls to zero when the AVS is inactive this could be seen in Fig. 11(top).

4. Conclusion

A novel predictive current control scheme for a HDPC is proposed which is simple in digital implementation and requires no additional circuitry. The proposed predictive current control scheme provides constant switching frequency of the AVS. Therefore, synchronization of switching can be obtained in order to provide sinusoidal supply currents. An AVS with a higher voltage is used in the HDPC to increase the average dc link voltage seen by the inversion stage. Therefore, a unity voltage transfer ratio can be achieved even at highly unbalanced supply voltage conditions. The average energy storage during a switching period in the AVS is maintained low by an appropriate control of the power flow. Thereby a

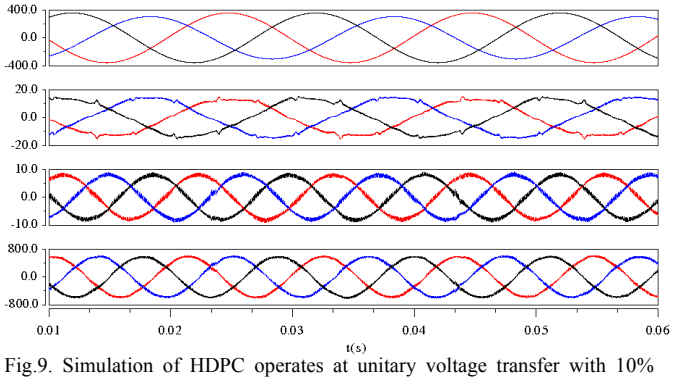

Fig.9. Simulation of HDPC operates at unitary voltage transfer with 10% supply voltage unbalanced (a) supply phase voltage, (b) supply currents, (c) load currents and (d) filtered line to line load voltage (Appendix).

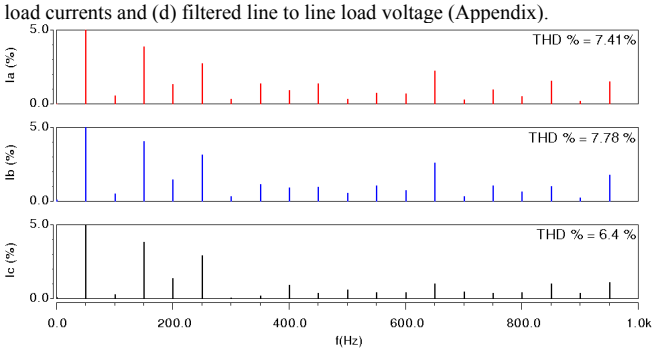

Fig.10. Supply current harmonics as a percentage of the fundamental when the HDPC demands unitary voltage transfer while the supply voltage is 10% unbalanced (Appendix).

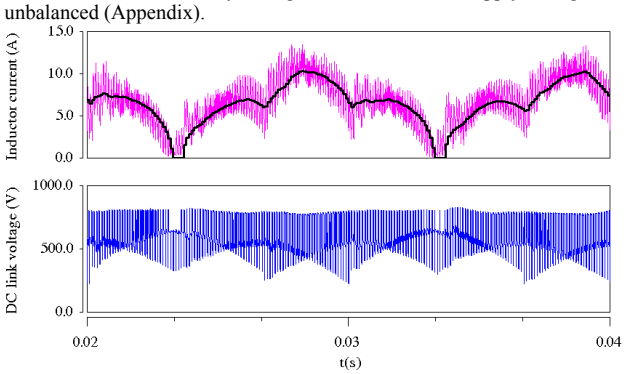

Fig.11. Simulation waveforms of HDPC utilizing a predictive current controller for the AVS when operating (a10% unbalanced supply voltage situation: (top) current through the AVS inductor i and its reference i^*, (bottom) DC link voltage seen by the inversion stage (Appendix).

quasi- direct power conversion is achieved for the AVS, which in conjunction to the lower power processed by the AVS means that the HDPC still preserves direct power conversion characteristics. The HDPC requires no additional clamp circuit which is usually used in the CMC for protection thereby reduction of cost for the clamp circuitry.

The proposed predictive current controller has offered a higher bandwidth control of the AVS as expected. Therefore acceptable amount of supply current harmonics has resulted even if the supply voltage is highly unbalanced.

Acknowledgement

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Appendix

The parameters used for the simulation results presented in Fig. 9, Fig. 10 and Fig. 11 are: $V_{in\text{-}phase}(rms)$ = 252.86V/216V/252.86V; $I_{in}(rms)$=9.57A/9.88A/10.08A; $V_{out\text{-}phase}$ (rms)= 240 V; f_{out} = 90 Hz; V_{AUX} =800 V; Supply Filter: L_{in}= 1 mH; C_{in} = 9.2 µF/phase; L_{AUX} = 3.15 mH; C_{AUX}= 20 µH; R_{load}=42 Ω; L_{load}= 5 mH/phase; f_{sw} =10 kHz.

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